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Semiconducting-Enriched Printed Carbon Nanotube Mat used for Fabrication of Thin Film Transistors

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***Abstract*-Semiconducting nanotubes, theoretically, offer great promise for a variety of applications in RF and microwave electronics. In this work, we present device performance of thin-film transistors fabricated using a spin-coating purified all-semiconducting nanotubes that is economical and lends itself to mass manufacturing of nanotube electronics.**

I. INTRODUCTION

Theoretically it's been proven, in 2004, that carbon nanotube devices have the potential to reach to the THz cutoff frequencies [1]. Since then, there have been many efforts to make this dream come true. However, only recently have the device cutoff frequencies crossed into the GHz range, as reviewed in [2]. Results from previous works show that having purified semiconducting tubes, as the channel of the transistor will properly lead to desired result however, to date, no RF devices with all-semiconducting nanotubes have been demonstrated. In this work, we present progress towards RF devices using all semiconducting nanotubes as the starting material. A spin-on process, which is compatible with standard semiconductor processing, is presented. The device performance is measured in an RF compatible electrode geometry. DC analysis of device characterization shows a high mobility and good on/off ratio in the range of more than 10^3 and 10^4 in some cases.

II. FABRICATION

A. Nanotube Mat, Chemical Process

Nanotube solution with 90% semiconducting nanotubes prepared using density gradient separation is used as the starting material for the device fabrication [3]. The protocol used for the dispersion of each sample is as follows:

1. 5% w/v solutions of surfactants were prepared in DI water.
2. 5 mg of nanotube sample was dispersed in 10 mL of surfactant solution.
3. Suspensions formed after addition of nanotubes were then sonicated for 3 hours.
4. Mixtures were then centrifuged at 16,400 rpm (@ 30 °C) for 1 hour, 6 times repeatedly.
5. Dispersions obtained after 6 times centrifugation were then used for the deposition.

Prior to the deposition of nanotubes, a Si/SiO_2 wafer was modified with APTES. For this modification wafers with thin oxide layers were first treated with hot piranha solution for 1 hour and then washed thoroughly with DI water. Piranha treatment introduces –OH groups on the oxide surface. For forming a thin monolayer, APTES was then poured onto these wafers kept under inert atmosphere. Excess APTES was removed by tilting the wafers vertically. After an hour wafers were washed with dry toluene and further sonicated in dry toluene for about a minute and then dried by blowing air. Nanotube solution was then either spin-coated or poured vertically on these wafers. Wafers were further air dried before observing them in an SEM (Fig. 1).

B. Transistor Fabrication

Following the nanotube deposition, the wafer was pattern for Source and Drain deposition using standard photolithography and Shipley photoresist. The mask was designed in an RF compatible electrode geometry. Also to study the effect of gate length on mobility, on/off ratio and RF properties, devices different gate lengths (5~100 micrometer) were designed in the mask. In all devices the gate width is fixed and 200

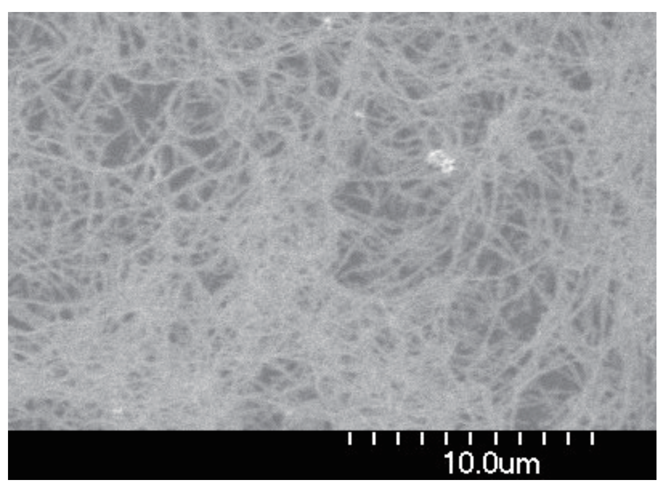

Figure 1. SEM image of CNT mat using APTES

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micrometer.

In the next step e-beam evaporation was used to deposit source and drain electrodes (10 nm Pd/ 40 nm Au). The Si wafer acts as the back gate and 300 nm of thermally grown SiO_2 was used as the gate dielectric. This design will allow for top-gate, three-terminal RF probing in the next generation of devices.

III. ELECTRICAL MEASUREMENTS

Following the fabrication of the device, we need to measure the electrical characteristics of it. DC measurement was done to study the mobility and on/off ratio of the fabricated device according to different parameters.

The I_D-V_D extracted from the dc measurement is shown in Fig. 2. Our results show that the I_D-V_D curve is linear for V_D between 1 V and -1 V, indicating good ohmic contact between nanotube and electrodes. By applying more negative V_D the devices clearly show saturation behavior as (Fig. 2).

The on/off ratio is more than 1000 in almost all devices. A reasonable assumption states that OFF current is roughly corresponding to the metallic nanotubes while both semiconducting and metallic tubes contribute in the ON current. Since we are using purified all-semiconducting (90% semiconducting) tubes in the channel, we are expecting high on/off ratio, which is true in our devices. In addition, the devices have a great p-type transistor response to the change in the back-gate voltage, which also is a result of forming the channel with semiconducting tubes. Gate voltage has been changed in the range of -10V to 10V with 2V increments.

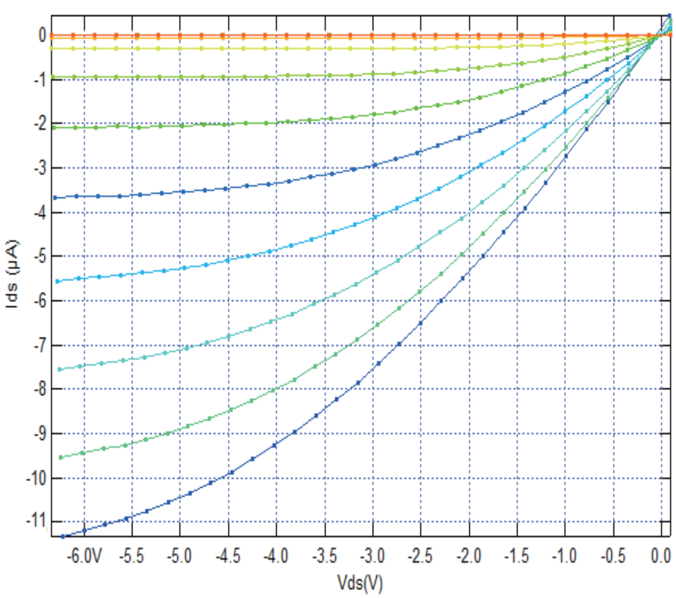

Figure 2. DC characteristic of the device showing the saturation behavior (V_g varies from -10V to 10V with 2V increment).

Mobilities up to ~30 cm^2/V-s are observed using conventional MOSFET equations and curve fitting the I_D-V_D characteristic. These devices clearly show potential for RF performance when suitably optimized.

IV. CONCLUSION

In summary we reported thin film transistors fabricated using semiconductor-enriched carbon nanotubes. The APTES chemical treatment of the surface also allowed selective deposition of semiconducting nanotubes on the surface. The dc electrical measurements show a great improvement in terms of mobility, current density and transconductance compared to previous works. Pushing this technology into the microwave (GHz) range will require shorter gate lengths and higher mobilities. Since these are some of the first spin-on, all semiconducting nanotube devices ever made, these initial results are indeed quite promising for RF and microwave electronics.

ACKNOWLEDGMENT

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