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Fundamental Limits on the Mobility of Nanotube-Based Semiconducting Inks

By *Nima Rouhi*,* *Dheeraj Jain*, *Katayoun Zand*, and *Peter John Burke*

Carbon-nanotube-based semiconducting inks offer great promise for a variety of applications including flexible, transparent, and printed electronics and optics. A critical drawback of such inks has been the presence of metallic nanotubes, which causes high-mobility inks to suffer from poor on/off ratios, preventing their applications in a wide variety of commercial settings. Here, we report a comprehensive study of the relationship between mobility, density, and on/off ratios of solution-based, deposited semiconducting nanotube ink used as the channel in field effect transistors. A comprehensive spectrum of the density starting from less than 10 tubes μm^{-2} to the high end of more than 100 tubes μm^{-2} have been investigated. These studies indicate a quantitative trend of decreasing on/off ratio with increasing density and mobility, starting with mobilities over 90 $cm^2\ V^{-1}s^{-1}$ (approaching that of p-type Si MOSFETs) but with on/off ratios ~10, and ending with on/off ratios $>10^5$ (appropriate for modern digital integrated circuits), but with mobilities ~1 $cm^2\ V^{-1}s^{-1}$. These studies provide the first important roadmap for the tradeoffs between mobility and on-off ratio in nanotube based semiconducting inks.

Single-walled carbon nanotube (SWNT) based semiconducting inks may have a wide variety of applications in printed electronics (such as inkjet printing,[1] role to role gravure,[2] and pad/screen printings[3]) as well as offering the possibility of heterogeneous integration of different semiconductor technologies such as Si CMOS, III-V, and optical display technologies. Recent progress in purification techniques[4] has lead to the prospect of all-semiconducting SWNT inks for unsurpassed performance in printed circuits.

In general, it is known that the mobility of individual, pristine semiconducting nanotubes can be up to 10 000 $cm^2\ V^{-1}s^{-1}$.[5] However, mobilities for random networks of carbon nanotubes has hovered until recently around the 1 $cm^2\ V^{-1}s^{-1}$ limit.[6] What sets the mobility of a random network of semiconducting nanotubes in relationship to individual nanotubes? Can the mobility be increased by increasing the density? How does this affect the on/off ratio and what are the physical processes that set limits on this scaling?

The most obvious reason that networks have lower mobilties than individual nantoubes is that tube–tube crossings limit the current flow from source to drain if the channel length is longer than the nanotube length. Increasing the network density can increase the current (and hence potentially the mobility).

However, the complexity of such a system, coupled with the presence of metallic nanotubes that can short-circuit the device if the density exceeds the percolation threshold, means that there is no general theory that explains quantitatively the relationship between mobility, density, and on/off ratio, so that phenomenological experimental approaches are necessary for progress in the field.

Although solution-based processing techniques enable the use of presorted semi-enriched nanotubes, limitations are imposed due to the fact that it is almost impossible to get cost-effective 100% pure semiconducting nanotubes in solution. Therefore, all semi-enriched solutions available on the market so far contain some amount of metallic nanotubes, which may impact semiconducting device properties. Other physical effects include the type of surfactant used in the nanotube ink suspension, deposition process (e.g. spin-on, ink-jet printed, drop-drying, gravure), wafer treatment used prior to nanotube deposition, and nanotube modification chemistry after deposition.

To date, there have been several research studies on parameters affecting the performance of the single-walled carbon nanotube field-effect transistors. However, most such studies use grown in-place SWNTs as the base material, which is not suitable for low-temperature substrates used in printed electronics, and also lacks a well-established prototype for growing all-semiconducting nanotubes.[6c,7]

Although it is known that in general the transconductance and on/off ratio of solution-processed nanotube transistors is highly related to the density of the tubes in a solution containing a mixture of metallic and semiconducting tubes,[6c,8] no such experimental studies have been performed on purified all-semiconducting nanotubes, which would also include the control over a wide range of different densities and in detail the effect of each density point on the mobility and on/off ratio. Snow et al. showed solution-based deposition of nanotubes on a polymeric substrate that suffers from a low on/off ratio because they used a mixture of metallic and semiconducting nanotubes in their solution.[8,9] Also, their study shows no control over the density and its effect on the mobility and on/off ratio of the device. In another study, Hu et al.[10] also demonstrate the effect of three different density points only on the sheet resistance of the nanotube networks using a novel filtration method, where – same as previous works – they used a mixture of metallic and semiconducting tubes. In addition, the nanotubes were deposited merely on filtering membranes, which are not the desired substrates for electronic applications. Other similar works show different deposition methods to have dense and aligned nanotube networks, while they as well use the mixture solution of nanotubes and utilize a spin-on method that is not compatible

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with printed electronics.[11] However, none of these research studies were able to demonstrate a systematic study on density control to find the extremes for different applications furthermore, they use the mixture of metallic and semiconducting nanotubes in the solution as the base material. Recently, there have been interesting investigations on purified all-semiconducting nanotube inks deposited on the substrate for fabrication of CNTFETs.[6a,6d]

So far, a systematic study of the relationship between the mobility, density, and on/off ratio of SWNT-based semiconducting inks has not been reported, especially for the extreme limits on density at the high and low end. These are the key technical factors (in addition to cost, which is not addressed in this paper) in determining if and when semiconducting-nanotube-based inks will ever find commercial applications.

In this work, we address for the first time the density scaling of mobility and on/off ratio in all-semiconducting nanotube deposited material experimentally, and mainly towards the end limits for the density variation so that it would be suitable for different electronic applications. Purified 99% semiconducting nanotubes in solution, "IsoNanotubes-S 99%" (commercially supplied by NanoIntegris, Inc.), were used as the base material. Another solution containing 90% semiconducting tubes has also been utilized, from the same provider, to explore the impact of the purity in highly purified inks. The ratio of semiconducting tubes in the solution was determined by the commercial provider using spectroscopic techniques, although we are not attempting to verify that ratio by the means of electrical measurements. However, the main goal of purification is to result in better electrical properties, which have not (until our work now) been carefully correlated with the spectroscopically determined fraction of semiconducting nanotubes. Here, we have addressed quantitatively and systematically this crucial and fundamental relationship between the purity (measured spectroscopically) and the mobility and on/off ratio. A full range of the density starting from 10 tubes μm^{-2} to the high extreme of more than 100 tubes μm^{-2} has been investigated. For the first time, this study carefully maps the relationship between density, mobility, on-off ratio, and spectroscopically determined purity, which lays the foundation for and opens up a wide range of applications of semiconducting nanotube inks in printed electronics.

Prior to the deposition of nanotubes, silicon substrates with 300 nm oxide layers (Si/SiO_2) were modified by 3-Aminopropyltriethoxy Silane (APTES) to form amine terminated self assembled monolayers (SAM). In order to achieve these monolayers, wafers with oxide layers were first treated with piranha solution for 1 hour at 100°C. Piranha treated wafers were then thoroughly washed with DI water and dried by blowing compressed air. Piranha-solution-cleaned wafers were dipped into an APTES solution in 2-propanol for 1 hour for surface functionalization. Wafers were then thoroughly washed with 2-propanol and air-blown dried. For having different amounts of modifications i.e., to have several different adsorption densities we used three different concentrations (1, 2, and 10%) of APTES solution in 2-propanol. Using the higher concentration (>10% in isopropanol) resulted wafers with uneven surfaces that were not suitable for the device fabrications. Using 1% or 2% solutions yielded much more uniform nanotube network densities.

A semienriched solution (90% or 99%) was used to deposit SWCNTs onto APTES modified wafers. Wafers were first masked with a PET film and Krypton tape to leave 1 cm^2 open blocks. 20 μL of nanotube solution was then placed in each block and left for adsorption for 1 hour. Excess nanotube solution was then washed with DI water and wafers were air-blown dried. To achieve several different densities of nanotubes, we used three different concentrations (0.005, 0.01, and 0.1 mg mL^{-1}) of nanotube solution. Each solution was used for the deposition on APTES modified wafers having different adsorption densities. **Figure 1** provides SEM images of the deposited nanotubes.

In order to achieve a range densities of nanotubes on wafers, we chose to vary two important factors related to the deposition process – (a) variations in the amount of surface modification by using APTES/isopropanol solutions with different concentrations and (b) changing the solution concentration of nanotubes used for deposition. Keeping one factor same at a time and varying the other factor resulted devices with several different distributions of nanotubes.

Solution-processed separations of nanotubes generally involve the use of surfactants to solubilize raw nanotube mixtures in DI water or other solvents before further processing. The concentration of nanotube dispersions highly depends on the surfactant used. For the most widely used surfactant sodium dodecyl sulfate (SDS), the maximum concentration is

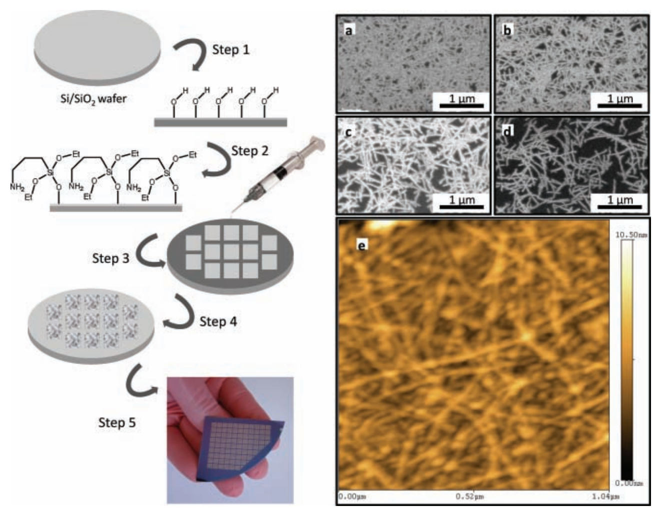

Figure 1. On the left: Deposition protocol. A schematic diagram of all semiconducting nanotube device fabrication. SiO_2 coated Si wafer was first treated with warm piranha solution that introduces –OH groups to the oxide surface (step 1), wafers were then introduced to APTES/Isopropanol solution for surface modification (step 2) by self-assembled monolayer (SAM) of amine terminated silane (APTES), on these modified wafers 1 cm^2 blocks were created using a PET film mask with pre-cut 1 cm^2 blocks, 20 μL of semi-enriched nanotube solution was dropped into each of these blocks (step 3). Wafers were then air dried (step 4) prior to electrode deposition onto them (step 5). On the right: SEM images of devices having different densities of nanotubes, nanotubes count estimated by visual inspection of SEM images for each of these device are 85, 50, 25, and 10 per μm^2 for devices shown in figures 1a, 1b, 1c, and 1d, respectively. Figure 1e shows a representative AFM image of nanotube network deposited on wafers.

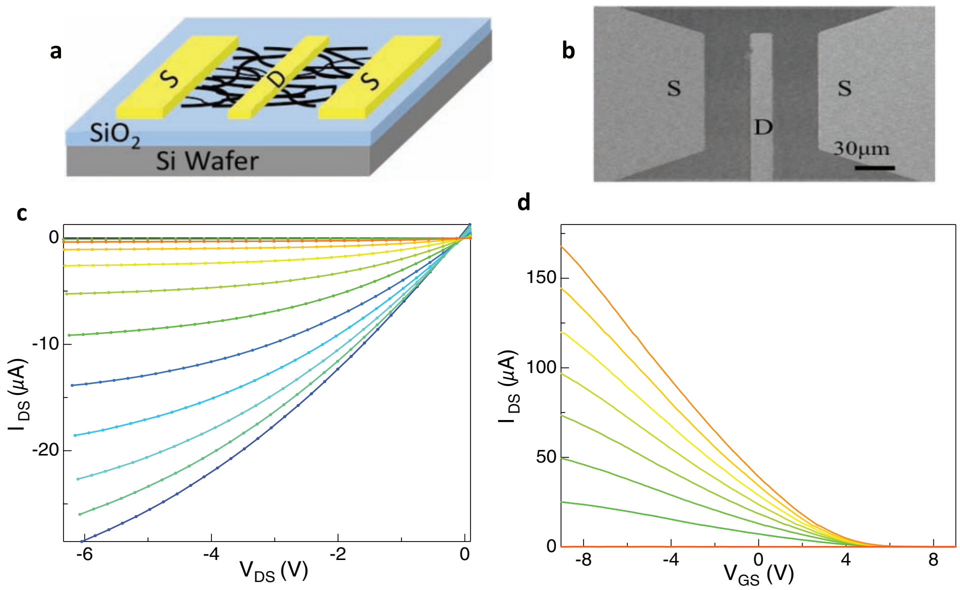

Figure 2. Electrical characteristics. a) Schematic diagram of the device with 300 nm thermally grown dry silicon-dioxide on top of a Si wafer and Pd/Au (15/30nm) source and drain electrodes for ohmic contact with random networks of the semiconducting nanotubes. b) SEM image of the device showing the channel area with drain electrode in the middle, channel width of 200 μm and channel length ($L_{channel}$) varying from 10 μm to 100 μm. c) Current–voltage characteristic of a device with channel length of 100 μm and W = 200 μm for different gate voltages ranging from +10 V to −10 V in 2 V steps, showing the expected saturation behavior at negative gate voltages and high drain-source voltage (V_{DS} changes from 0 V to 6 V). d) Depletion curve (I_D–V_G) of a device with channel length of 100 μm and drain-source voltage changing from 0 to 7 V.

reported to be around 0.12 mg mL^{-1},[12] although when these solutions are further processed for purification and separation, only a fraction of nanotubes compared to the starting solution are left in the resultant solution. In our experiments, we varied the nanotube concentration until just prior to precipitation, and also via dilution until no nanotubes were visibly deposited. When the solution was diluted to 0.001 mg mL^{-1}, after deposition very few nanotubes were found on wafers for any amount of surface modification. On the other hand, increasing the concentration up to 0.1 mg mL^{-1} (by evaporative drying) resulted in precipitation of nanotubes from the dispersion. In this way, we were able to control the entire possible range of nanotube concentrations in the ink prior to deposition, in order to investigate their effects on the final mobility, deposited density on the wafer, and on/off ratio.

Based on visual inspection of SEM images obtained from different locations on each channel for every device, number of nanotubes was counted in a 1 μm^2 area. Images taken at different locations for each channel show a very uniform nanotube-network channel (Supporting Information, Figure S3). Tube densities (D) ranging from 10 to 100 tubes per μm^2 were deposited to investigate the impact of tube density on both the mobility and the on/off ratio.

Nanotube devices in a back gate configuration with channel lengths ranging from 10–100 μm (with 10 μm increments) were fabricated. 300 nm thermally grown oxide cap is used as the insulating layer for the back gate Si substrate. In all the devices, the gate width is fixed at 200 μm. Source and drain electrodes (15 nm Pd/30 nm Au) were deposited using e-beam evaporation followed by a lift-off process and photolithography.

Figure 2 shows the schematic and SEM image of a fabricated device, as well is I_D–V_D curves and depletion curves. The $I_D - V_D$ curve is linear for V_D changing between +1 V and −1 V, indicating good ohmic contact between the nanotubes and the electrodes (Supporting Information, Figure S1). By applying more negative V_{DS} the devices clearly show saturation behavior (Figure 2c). The devices exhibit p-type behavior, consistent with prior work on nanotube networks.

Using the conventional I–V equations for MOS devices in triode region, we calculated the mobility using

$$\mu = \frac{L}{W}\frac{1}{C_{ox}}\frac{1}{V_{ds}}\frac{d\,I_{ds}}{V_{GS}} \tag{1}$$

where L is the channel length, W the channel width, and C_{ox} the capacitance per unit area between the gate and the nanotube network. For calculation of the capacitance, we used the parallel plate estimate. Strictly speaking, this is not correct, because this method overestimates the oxide capacitance (and hence underestimates the mobility) when the network density is low. For aligned arrays, the capacitance per unit area is given by[13]

$$C = \left\{C_Q^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_{ox}}\ln\left[\frac{\Lambda_0}{R\pi}\sinh\left(\frac{2\pi t_{ox}}{\Lambda_0}\right)\right]\right\}^{-1}\Lambda_0^{-1}, \tag{2}$$

where t_{ox} is the oxide thickness (300nm in our case), and Λ_0 is the tube-tube separation. For random arrays, Equation 2 is expected to be a qualitative guide, but not to hold quantitatively. When the nanotube-nanotube spacing becomes comparable to the dielectric thickness, the parallel plate capacitance formula deviates from Equation 2. In our experiments, with average nanotube lengths 1 ~ 5 μm, and areal densities of 10–100 nanotubes μm^{-2}, we expect that the parallel plate capacitance underestimates the actual capacitance by about 30% for the lowest densities we use, and less so for the higher densities. Therefore, our use of the parallel plate capacitance for estimating C_{ox} is justified.

Using this technique, we find our devices have mobilities ranging from 1–90 cm^2 V^{-1}s^{-1} (if we use Equation 2 for low density samples to estimate the capacitance). The highest mobility devices have in fact higher mobility than any published nanotube network device fabricated from purified (semi-enriched) SWNT devices, indicating that we are successfully probing the ultra-dense limit of SWNT devices.

Although the mobility should be a bulk property (independent of device length and width), because of the presence of metallic nanotubes and percolation effects, it has been commonly observed in as-grown nanotube networks (containing roughly 1/3 metallic and 2/3 semiconducting nanotubes) that the mobility does in fact depend on gate length. This effect has been reproduced in simulations of random networks, taking the 1/3 metallic nanotubes into account.[6c] Recently this length dependence was also observed for nanotube networks containing purified nanotubes.[6d] In our work we also find a length dependence to the mobility, on current, and transconductance, as shown in **Figure 3**. The overall scaling with length does not depend strongly on the purity of nanotube starting material, as shown in Figure 3a.

The on/off ratio is more than 1000 in most of the devices, especially the ones with longer gate lengths, leading us to the conclusion that the surface treatment will also help us with the deposition of semiconducting tubes although the solution was 99% semiconducting enriched already. Study of the on/off ratio showed that 20 μm is a turning point for on/off ratio. For most of the devices with the gate length of more than 20 μm, the on/off ratio is more than 1000 while for smaller gate lengths this can come below 100 in some cases. A reasonable assumption states that OFF current is roughly corresponding to the metallic pathways from source to drain while both semiconducting and metallic tubes contribute in the ON current. The highest on/off ratio we observed was around 110 000.

In **Figure 4a**, we plot the mobility versus nanotube density. The only varying parameter was the tube density. Different nanotube densities were obtained by controlling the density in the solutions, as discussed above. This allowed us to systematically evaluate the effect of nanotube density on mobility. It is clear from the plot that increasing the density increases the mobility. While this is consistent with prior reports on random arrays of as-grown (1/3 metallic and 2/3 semiconducting tubes) and simulations of such systems,[6c,6d] this is the first systematic study of this effect on purified all semiconducting devices.

The on/off ratio is also a very important parameter, in particular with relation to digital switching and low power applications. In Figure 4b, we plot the mobility as a function of the on/off ratio. For a given gate length, we observe a very clear trend of the on/off ratio with mobility, starting with mobilities over 90 cm^2 V^{-1}s^{-1} (approaching that of p-type Si MOSFETs) but with on/off ratios ~10, and ending with on/off ratios >10^5

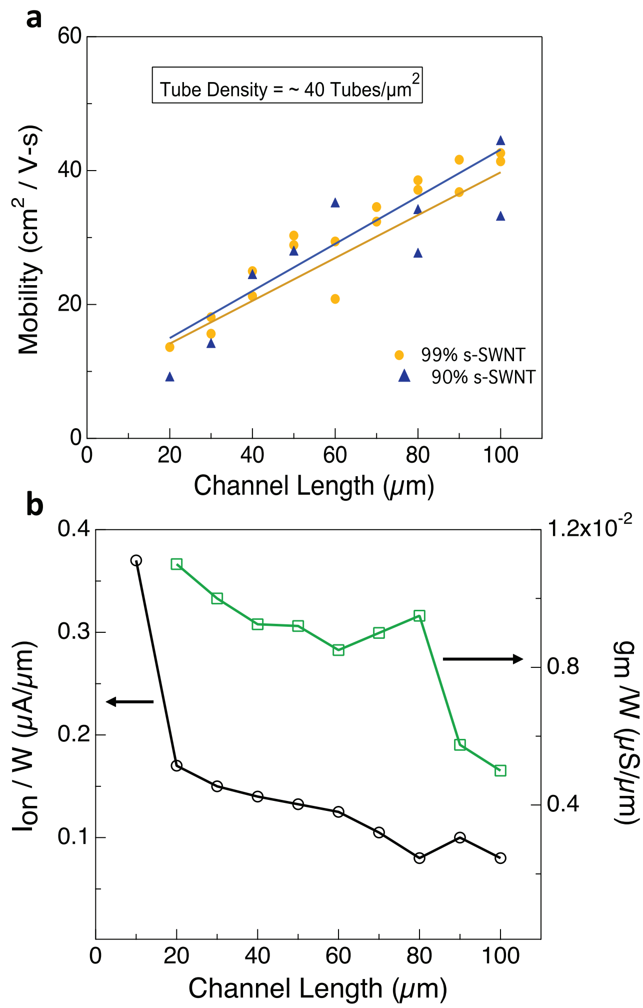

Figure 3. Channel length impact. a) Mobility vs. channel length for $L_{channel}$ = 20 μm to 100 μm. As a sample, the measurements were performed on devices with the moderate tube density of around 40 tubes per μm^2 and for 2 different semiconducting to metallic ratios in the solution. Tube density was controlled both by the surface modification and the density in the solution. b) Current density vs. channel length (W is fixed at 200 μm) on the left axis shows a decrease in I_{on} as the channel length increases to 100 μm. The right axis demonstrates the transconductance per unit width (g_m/W) decreases by increasing the channel length.

(appropriate for modern digital integrated circuits), but with mobilities ~10 cm^2 V^{-1}s^{-1}.

The increase in overall nanotube density will also increase the density of metallic nanotubes. When the semiconducting nanotubes are all gated off, the background conduction of metallic nanotubes will depend in a non-trivial way on the density due to percolation effects. Increasing the overall density will increase the metallic density, which will increase the off current. Similarly, increasing the overall density will increase the on current, due simply to the increased number of tubes. However, the effect of the density on the on/off ratio is much more difficult to predict theoretically. While simulations can attempt to reproduce the features, there is no substitute for a quantitative, systematic study of the effects of

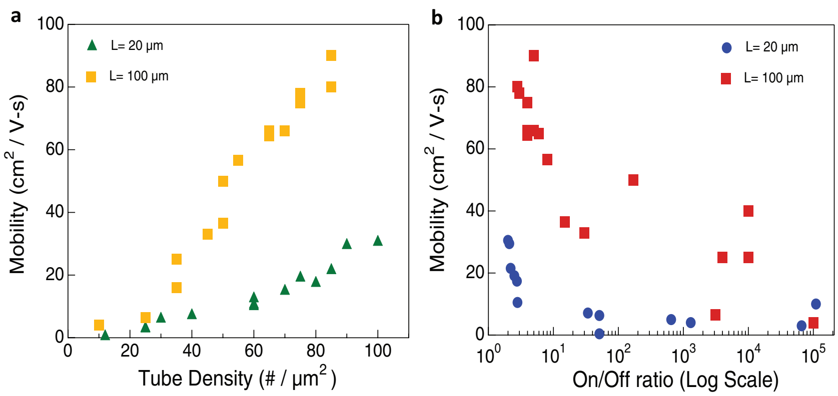

Figure 4. Mobility and on/off ratio. a) Mobility as a function of nanotube density for lower and upper channel length extremes ($L_{channel}$ = 20 μm and $L_{channel}$ = 100 μm). Tube density was controlled and calculated as described in the text. Mobilities of around 90 $cm^2 V^{-1} s^{-1}$ were achieved at the high-density limit of nanotube deposition and the channel length of 100 μm, and W = 200 μm. b) Mobility as a function of on/off ratio showing the inverse relationship for the same devices in (a). The highest on/off ratios correspond to the lowest tube densities and therefore, low mobilities and vice versa.

density on on/off ratio and mobility, which we have presented in Figure 4b.

While we have clearly studied all-semiconducting nanotube solutions as inks for printed electronics, several issues need to be addressed before such inks are practical. First, the drying time should be reduced, and this will impact the final SWNT density (and hence mobility, according to our studies). Whereas we have used a drying time of 1 hour, ideally the drying time will be less than 5 seconds for both ink-jet and gravure type printing. Heating during printing may aid this process somewhat. Secondly, the deposition on other substrates (such as PTFE) should also be investigated. Finally, the cost of the inks needs to be evaluated, in systematic comparison with competing, lower-mobility inks for each application.

In summary we have reported thin-film transistors fabricated using semiconducting-enriched carbon nanotubes. The ratio of semiconducting tubes in the solution was determined by the commercial provider using spectroscopic techniques. Substrate surface modification using APTES prior to nanotube deposition facilitated selective deposition of semiconducting nanotubes on the surface. By changing the modified surface morphology and varying the nanotube solution concentrations to their end limits, we were able to obtain the nanotube densities on wafers that are practically feasible with commercially available resources.

We studied the dependence of mobility on the nanotube density over the channel, which shows a linear relationship. However, it may saturate at a threshold point because of the increase in intertube junction resistance. Moreover, the inverse correlation of the on/off ratio and tube density and also the effect of density on the mobility can lead us to the inverse change in on/off ratio according to change in the mobility, which is supported by the experimental data.

This work lays a clear roadmap for applications of nanotube-based semiconducting inks in printed electronics. Practitioners and circuit designers can now quantitatively study the trade-off between mobility and on/off ratio in systems designs, and adjust the nanotube density for optimum system performance. Prior to our studies, this was done on a hit/miss type basis.

We have not reached the fundamental limits of mobility. Average tube length and average tube diameter have not been adjusted in this process. With optimization, the fundamental limits are expected to improve and eventually allow printable, scalable high-throughput processes for unprecedented technology opportunities such as wearable electronics, high-efficiency solar cells printed on flexible surfaces, implantable biosensors, and other future applications enabled by high-performance flexible electronics.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] W. R. Small, M. I. H. Panhuis, *Small* **2007**, *3*, 1500.
[2] M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, J. M. Tour, G. Cho, *IEE Trans. Electron Devices* **2010**, *57*, 571.
[3] W. B. Choi, D. S. Chung, J. H. Kang, H. Y. Kim, Y. W. Jin, I. T. Han, Y. H. Lee, J. E. Jung, N. S. Lee, G. S. Park, J. M. Kim, *Appl. Phys. Lett.* **1999**, *75*, 3129.
[4] M. C. Hersam, *Nat. Nanotechnol.* **2008**, *3*, 387.
[5] X. J. Zhou, J. Y. Park, S. M. Huang, J. Liu, P. L. McEuen, *Phys. Rev. Lett.* **2005**, *95*, 146805-1.
[6] a) N. Rouhi, D. Jain, K. Zand, P. J. Burke, in *Proc. IEEE IMS*, IEEE, Anaheim, **2010**, p. 1420; b) C. Rutherglen, D. Jain, P. Burke, *Nat. Nanotechnol.* **2009**, *4*, 811; c) Q. Cao, J. A. Rogers, *Adv. Mater.* **2009**, *21*, 29; d) C. Wang, J. L. Zhang, K. M. Ryu, A. Badmaev, L. G. De Arco, C. W. Zhou, *Nano Lett.* **2009**, *9*, 4285.
[7] a) U. J. Kim, E. H. Lee, J. M. Kim, Y. S. Min, E. Kim, W. Park, *Nanotechnology* **2009**, *20*; b) E. S. Snow, J. P. Novak, P. M. Campbell, D. Park, *Appl. Phys. Lett.* **2003**, *82*, 2145.
[8] E. S. Snow, P. M. Campbell, M. G. Ancona, J. P. Novak, *Appl. Phys. Lett.* **2005**, *86*.

[9] M. D. Lay, J. P. Novak, E. S. Snow, *Nano Lett.* **2004**, *4*, 603.
[10] L. Hu, D. S. Hecht, G. Gruner, *Nano Lett.* **2004**, *4*, 2513.
[11] a) M. A. Meitl, Y. X. Zhou, A. Gaur, S. Jeon, M. L. Usrey, M. S. Strano, J. A. Rogers, *Nano Lett.* **2004**, *4*, 1643; b) S. J. Oh, Y. Cheng, J. Zhang, H. Shimoda, O. Zhou, *Appl. Phys. Lett.* **2003**, *82*, 2521; c) J. U. Park, M. A. Meitl, S. H. Hur, M. L. Usrey, M. S. Strano, P. J. A. Kenis, J. A. Rogers, *Angew. Chem. Int. Ed.* **2006**, *45*, 581; d) X. L. Li, L. Zhang, X. R. Wang, I. Shimoyama, X. M. Sun, W. S. Seo, H. J. Dai, *J. Am. Chem. Soc.* **2007**, *129*, 4890; e) Q. Cao, S. H. Hur, Z. T. Zhu, Y. G. Sun, C. J. Wang, M. A. Meitl, M. Shim, J. A. Rogers, *Adv. Mater.* **2006**, *18*, 304.
[12] L. Y. Yan, Y. F. Poon, M. B. Chan-Park, Y. Chen, Q. Zhang, *J. Phys. Chem. C* **2008**, *112*, 7579.
[13] Q. Cao, M. G. Xia, C. Kocabas, M. Shim, J. A. Rogers, S. V. Rotkin, *Appl. Phys. Lett.* **2007**, *90*.

Supporting Information:

Fundamental Limits on the Mobility of Nanotube Based Semiconducting Inks

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Ohmic contact with nanotubes

Since nanotubes are intrinsically p-type, Pd is a proper metal to have ohmic contact to the nanotubes. To further investigate the ohmic contact between source-drain electrodes and nanotube network we studied the current-voltage relation for small V_{DS} shown in figure S1. As it can be seen, the I-V relationship is linear for V_{DS} changing from -1V to 1V (triode region) for four different gate voltages (+5V, 0V, -5V, and -10V).

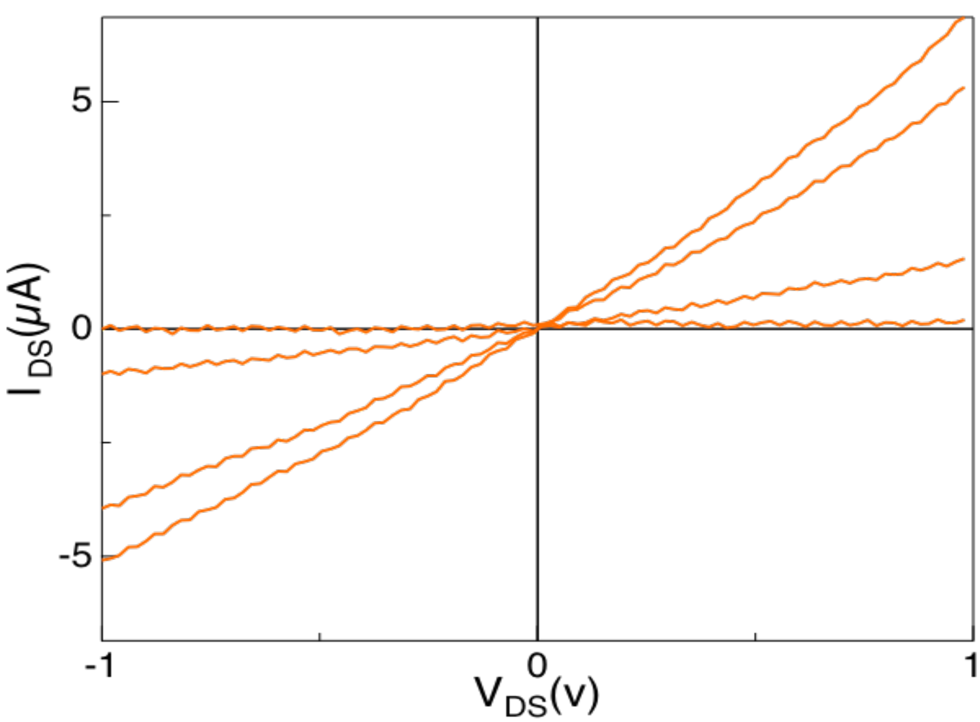

Figure S1 | Ohmic contact with electrodes. a, Current-Voltage characteristic for small V_{DS} changing from -1V to 1V with different gate voltages (+5V, 0V, -5V, -10V), L= 100μm and W= 200μm.

Hysteresis in the depletion curve

The depletion curves (I_D-V_G) show a certain amount of hysteresis as the drain voltage changes from 0V to 7V forward and backward. It's been demonstrated in figure S2 that the maximum voltage difference for a device with L= 100μm and W= 200μm, is around ΔV= 3.5V. The hysteresis can be reduced with better electrode contacts (thermally annealing the electrodes) and/or using high-K dielectrics.

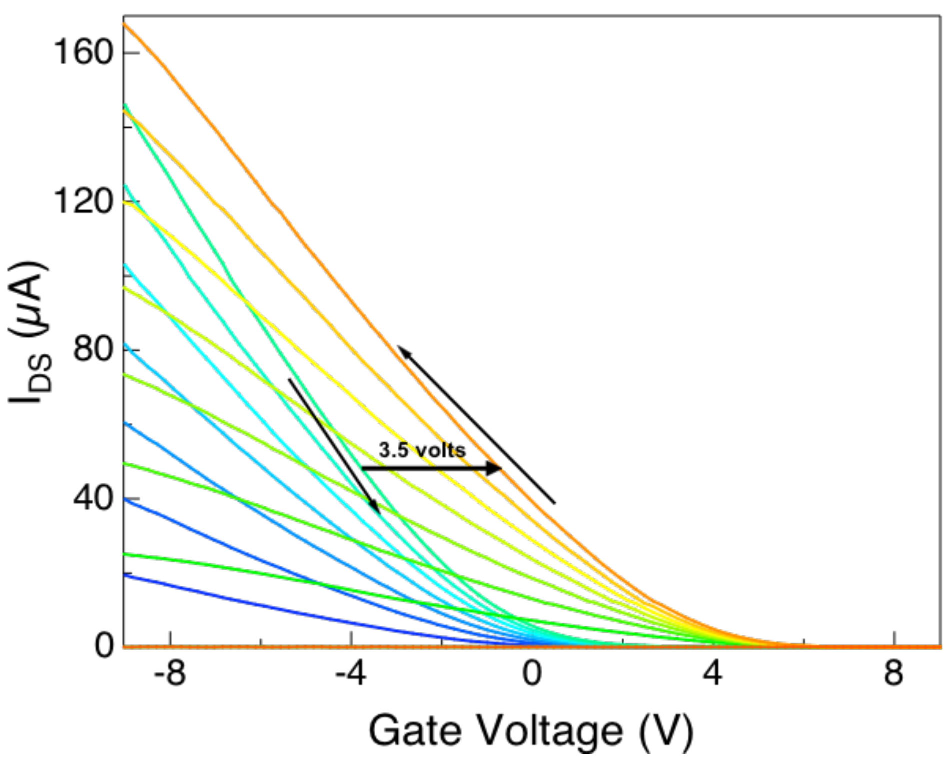

Figure S2 | Hysteresis in depletion curve. a, I_D-V_G for drain-source voltages from 0V to 7V with 1V increment and gate voltage changing from -10V to +10V with 2V increment steps.

Nanotube network uniformity

Obtaining a uniform channel is one of the most important issues especially with longer and wider channels when the goal is to print the nanotube network on large area panels. Figure S3 shows the SEM sample images taken from different device across the wafer and also on 4 different locations inside each device's channel.

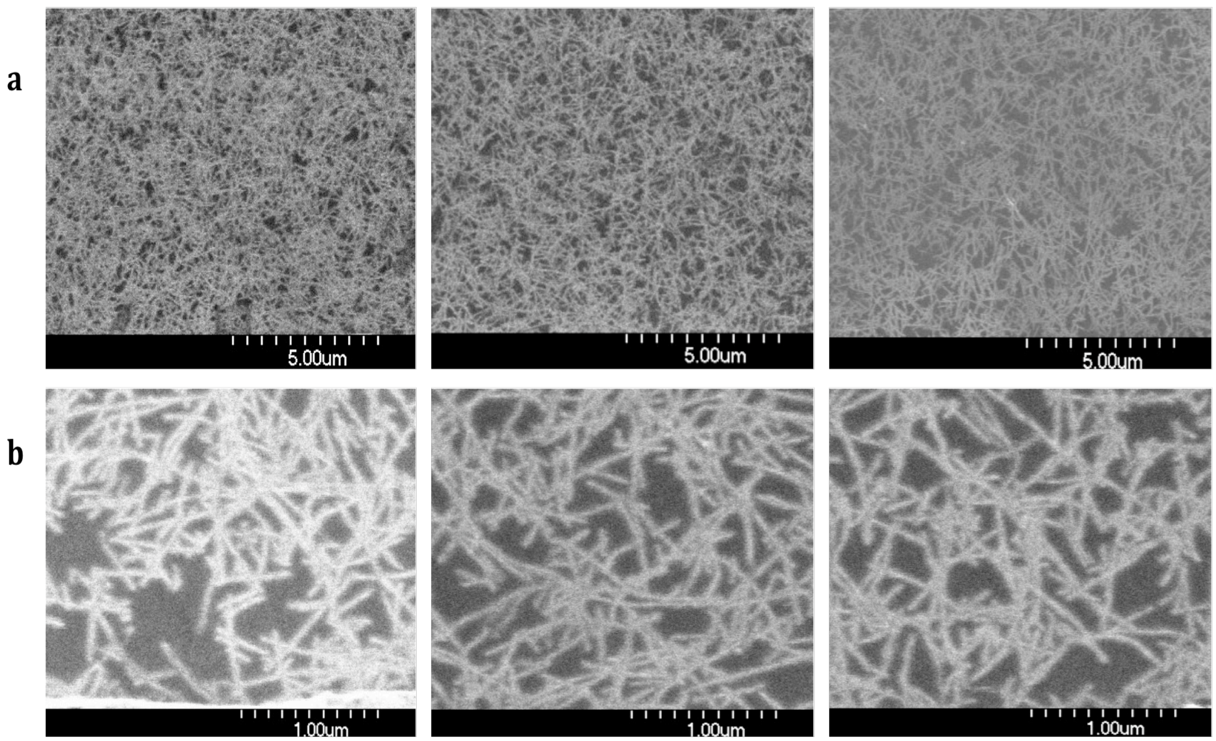

Figure S3 | Uniform density. a, Uniform density of three different devices on random location across the wafer. **b,** Uniform nanotube network in one of the devices in 3 different locations inside its channel.

Mobility vs. On/Off ratio Comparison

Other researchers have measured mobility and on/off ratio for various processes, although most with as-grown nanotubes containing a mixture of 1/3 metallic and 2/3 semiconducting nanotubes as the starting material, and modifying that ratio either during or after deposition. Their numbers are qualitatively in agreement with our study, although they are under a wide variety of conditions.

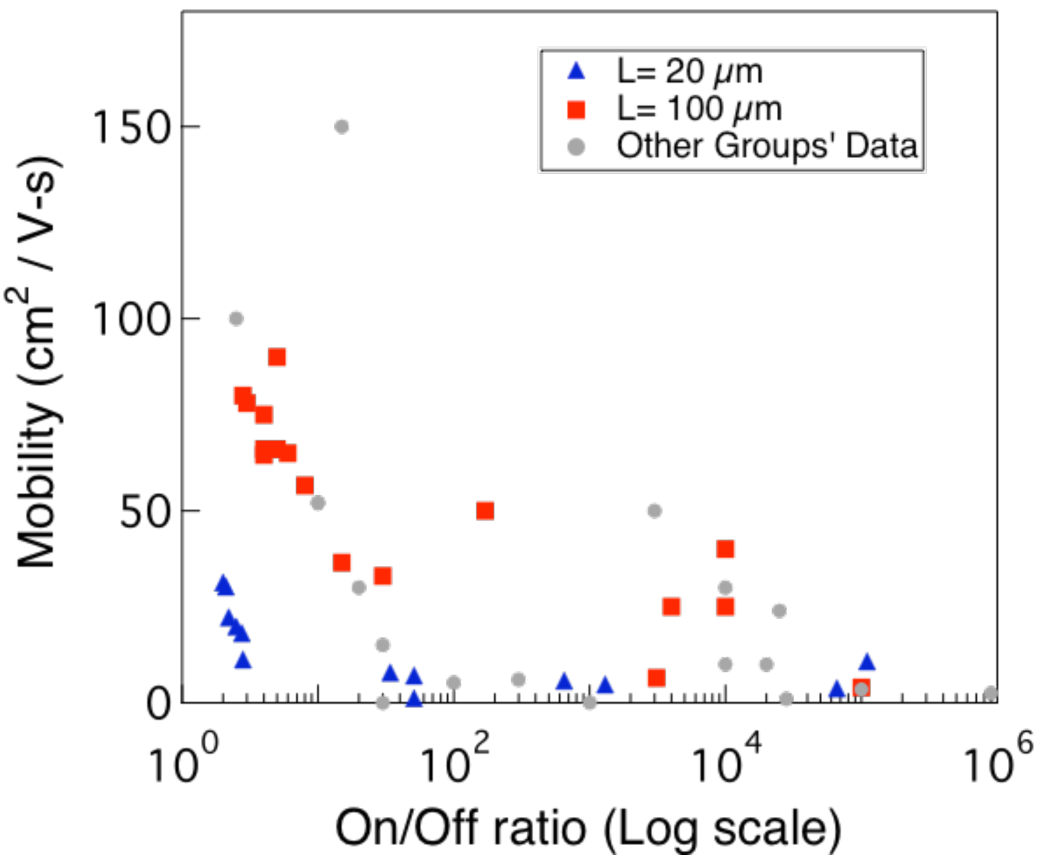

Figure S4 | Mobility and On/Off ratio comparison. Mobility as a function of on/off ratio for the same devices in figure 4 with the comparison to other research works so far in this area (gray dots).

Table S1. Mobility vs. On/Off ratio Comparison: Data points from figure S4; including all different data sets from our devices with channel lengths of 20 μm and 100 μm (channel width is 200 μm for all of our devices) and also other research works to date with different methods of depositing nanotubes from a solution.

Mobility [$cm^2\ V^{-1}\ s^{-1}$]	On/Off ratio	Reference
3	66000	This Work
5	650	This Work
22	2	This Work
19	3	This Work
4	1300	This Work
0.4	51	This Work
11	3	This Work
7	34	This Work
7	51	This Work
17	3	This Work
30	2	This Work
31	2	This Work
10	110000	This Work
57	8	This Work
66	5	This Work
90	5	This Work
50	170	This Work
40	10000	This Work
25	4000	This Work
7	3100	This Work
33	30	This Work
4	100000	This Work
25	10000	This Work

65	4	This Work
65	6	This Work
75	4	This Work
37	15	This Work
78	3	This Work
66	4	This Work
80	3	This Work
10	10000	[1][1]
6	300	
3.5	100000	[2][2]
2.5	900000	
0.03	1000	[3][3]
5.2	100	
150	15	[4][4]
1	28000	[5][5]
100	2.5	
15	30	
10	20000	
0.001	30	[6][6]
50	3000	
24	25000	
30	10000	[7][7]
30	20	
52	10	

Reference:

[1] M. Engel, J. P. Small, M. Steiner, M. Freitag, A. A. Green, M. C. Hersam, P. Avouris, *Acs Nano* **2008**, *2*, 2445.

[2] M. C. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim, Z. N. Bao, *Science* **2008**, *321*, 101.

[3] M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, J. M. Tour, G. Cho, *Ieee Transactions on Electron Devices* **2010**, *57*, 571.

[4] E. S. Snow, P. M. Campbell, M. G. Ancona, J. P. Novak, *Applied Physics Letters* **2005**, *86*.

[5] M. Kanungo, H. Lu, G. G. Malliaras, G. B. Blanchet, *Science* **2009**, *323*, 234.

[6] M. Ha, Y. Xia, A. A. Green, W. Zhang, M. J. Renn, C. H. Kim, M. C. Hersam, C. D. Frisbie, *Acs Nano* **2010**.

[7] C. Wang, J. L. Zhang, K. M. Ryu, A. Badmaev, L. G. De Arco, C. W. Zhou, *Nano Letters* **2009**, *9*, 4285.