Microwave nanotube transistor operation at high bias

Z. Yu, C. Rutherglen, and P. J. Burke[a)]
Integrated Nanosystems Research Facility, Department of Electrical Engineering and Computer Science, University of California, Irvine, California 92697-2625

(Received 5 September 2005; accepted 10 May 2006; published online 8 June 2006)

We measure the small signal, 1 GHz source-drain dynamical conductance of a back-gated single-walled carbon nanotube field effect transistor at both low and high dc bias voltages. At all bias voltages, the intrinsic device dynamical conductance at 1 GHz is identical to the low frequency dynamical conductance, consistent with the prediction of a cutoff frequency much higher than 1 GHz. This work represents a significant step towards a full characterization of a nanotube transistor for rf and microwave amplifiers. © *2006 American Institute of Physics*.
[DOI: 10.1063/1.2210447]

Theoretically, single-walled carbon nanotube field effect transistors (SWCNT FETs) are predicted to have intrinsic cutoff frequencies approaching the terahertz range.[1,2] Here "intrinsic" means that the parasitic capacitance due to fringing fields is negligible compared to the gate-source capacitance required to modulate the conductance. In practice, intelligent electrode geometries are required to minimize the fringing field parasitic capacitance to achieve this limit, for example, by using nanowires and nanotubes as the electrodes, as we suggested in.[1] In this letter, we take a significant step towards demonstrating the goal of a high frequency nanotube transistor by measuring the high dc bias small signal 1 GHz dynamical source-drain conductance of a back-gated SWCNT FET. Many theories have been developed to attempt to understand the complex phenomena of ac transport in nanoelectronic systems in the linear response regime where the ac and dc transports are qualitatively different.[3] (For example, is the conductance quantized in units of e^2/h at ac? The answer to this question is in general unknown.) Note that these theories do not necessarily involve Luttinger liquid physics, as the conductance at ac is predicted to deviate from e^2/h even for quantum point contact systems. (See, e.g., Ref. 4, where the gigahertz conduction of a quantum point contact is predicted theoretically to be dramatically different than the dc value.) In the face of this theoretical uncertainty, *experiment should be the guide!* This work takes the unprecedented step of *measuring* the ac properties of an *active, high bias* device, for which there is currently *no* theoretical model. The intrinsic device dynamical conductance at 1 GHz is identical to the low frequency dynamical conductance, consistent with the prediction of a cutoff frequency much higher than 1 GHz.

A full rf characterization of any three terminal device (including SWCNT FETs) requires the measurement of a matrix that relates the source ac voltage, the source ac current, the gate ac voltage, and the gate ac current.[5] This 2×2 matrix (called the h matrix, or equivalently the impedance matrix, or equivalently the S matrix) depends on the dc voltages at the source and gate, and on the frequency. In order to determine the cutoff frequency, the most commonly quoted figure of merit for any active device, one needs to measure the entire S matrix, including S_{11}, S_{12}, S_{21}, and S_{22}.[5] Simply measuring S_{12} is not sufficient to determine the cutoff frequency and is not sufficient to determine the gain of the device when used as an amplifier. For typical operating conditions in applications such as low-noise amplifiers (LNAs), one is most interested in the value of this matrix at a dc bias voltage in the range of saturation. This matrix determines the gain of the device in a practical circuit, as well as the input and output impedances, which determines what sort of external impedance matching circuits are needed on the input and the output.

We recently measured[6] one element of this matrix at 2.6 GHz for a SWCNT FET at cryogenic temperatures in the zero-dc source-drain bias range of operation. While our work demonstrated SWCNT FET operation at microwave frequencies, the zero-bias range of operation is not the most technologically relevant bias, especially for LNAs. In this letter, we present microwave measurements at the technologically relevant high dc bias voltage of the ratio of the ac source-drain current to the ac source-drain voltage, one element of the y matrix. (This can be considered the drain resistance in our recent model[1] and is important because it determines the output impedance of the device, which in turn determines the gain.) Using a technique to deembed parasitics,[7] we show that this ratio at 1 GHz is the same as it is at dc for the intrinsic device. This is a measurement of one of the elements of the S matrix at high bias for a SWCNT FET, a significant step towards a full characterization of the S matrix that sets the output impedance, input impedance, and ultimately the gain of a SWCNT FET.

Individual SWCNTs were synthesized via chemical vapor deposition according to previously published recipes[8] on oxidized, p-doped Si wafers with a 300–400 nm SiO_2 layer. Metal electrodes were formed on the SWCNTs using electron-beam lithography and metal evaporation of 30 nm Pd/20 nm Cr/100 nm Au trilayer.[9] The devices were not annealed. Nanotubes with electrode spacing of 1 μm were studied. Typical resistances were $\sim$100 kΩ; some nanotubes had resistances below 50 kΩ. In this study we focus on semiconducting SWNTs (defined by a gate response) with resistance below 50 kΩ. Measurements were performed at room temperature in air. We fabricated devices on two wafers. One of the wafers contains 32 devices, a yield of 70%, and an average resistance of 140 kΩ. The other wafer contains 30 devices, a yield of 60%, and an average resistance of 130 kΩ. Figure 1 shows a scanning electron microscope

[a)]Electronic mail: pburke@uci.edu

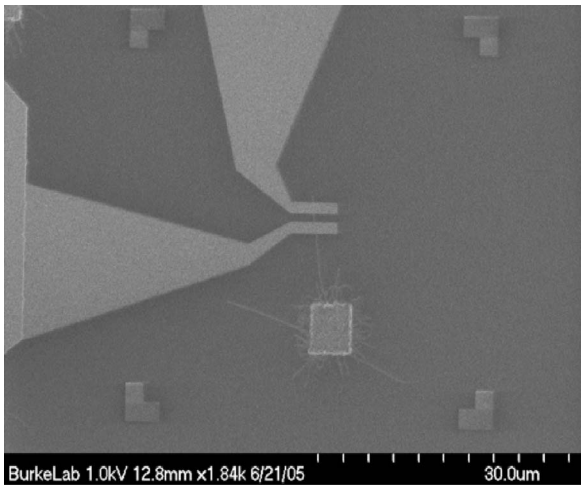

FIG. 1. SEM image of SWCNT FET.

(SEM) image of the SWCNT device presented in this letter; other devices showed a similar behavior.

Figure 2 shows the room temperature *I-V* characteristic of a SWCNT FET with a 1 μm source-drain spacing. Since this length is comparable to the mean free path, this device is in the quasiballistic limit at low bias, but in the diffusive regime at high bias. The low-bias resistance of this device was 47 kΩ. The inset shows the low-bias depletion curve, which displayed a *p*-type behavior.

In order to measure the dynamical impedance at microwave frequencies, we employed the same technique that we recently used to measure metallic SWCNTs.[7] A commercially available microwave probe (suitable for calibration with a commercially available open/short/load calibration standard) allowed for transition from coax to lithographically fabricated on chip electrodes. The electrode geometry consisted of one small contact pad of 50×50 μm^2, and the other of 200×200 μm^2. A microwave network analyzer is used to measure the calibrated (complex) reflection coefficient $S_{11}(\omega)\equiv V_{\text{reflected}}/V_{\text{incident}}$, where V_{incident} is the amplitude of the incident microwave signal on the coax, and similarly for $V_{\text{reflected}}$. This is related to the load impedance $Z(\omega)$ by the usual reflection formula: $S_{11}=[Z(\omega)-50\ \Omega]/[Z(\omega)+50\ \Omega]$. At the power levels used (3 μW), the results are independent of the power used.

As we discussed in quantitative detail in our work on metallic SWCNTs,[7] measurements of the absolute value of the microwave conductance of a high impedance device are

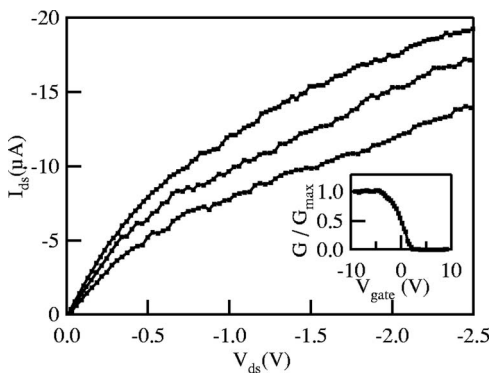

FIG. 2. Current-voltage characteristic at $V_{\text{gate}}=-8$, -7, and -5 V for SWCNT FET. Inset shows small bias depletion curve.

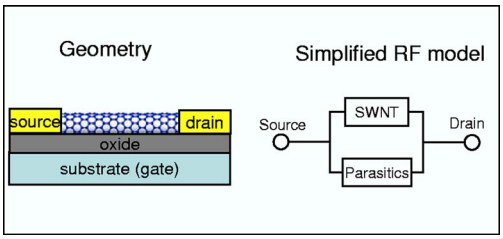

FIG. 3. Device geometry and rf model for interpretation.

generally associated with significant error bars. This is because of the difficulty in separating the inherent device performance from parasitics parallel with the device, as shown in Fig. 3. Unless extreme care is taken in the calibration, these parasitics are difficult to model and hence "calibrate out." However, *changes* in the device ac properties with dc bias are much clearer since the dc bias can be changed without the need to physically adjust the probes. This assumes that the parasitics do not change with the dc bias, which can easily be checked in a control experiment. In our experience, such control experiments are critical since in certain cases the doped semiconducting substrate can change its rf feedthrough properties depending on the electrode dc bias, which can easily be mistaken for intrinsic nanotube performance.

We plot in Fig. 4 the SWCNT FET dynamical conductance as a function of source-drain bias voltage for a fixed gate voltage of -8 V. The dc curve is obtained by numerically differentiating the measured *I-V* curve. The ac (1 GHz) curve is obtained by relating the change in the measured value of S_{11} to the change in the conductance through the formula $G(\text{mS})\approx1.1\times S_{11}(\text{dB})$.[7] A background parasitic conductance of $(3.37\times4)e^2/\text{h}$ was subtracted from G, which was determined using a control set of electrodes integrated onto the same wafer with no nanotube.

The changes in S_{11} with the source-drain voltage are systematic and reproducible. The change in S_{11} with source-drain voltage is not an artifact, since control samples without CNT bridging do not exhibit this effect. As such, this is a measurement of the dynamical impedance of a SWCNT FET at high bias. Our results clearly demonstrate that the 1 GHz intrinsic device performance (neglecting parasitics) is the same as the dc performance, indicating that the ultimate in-

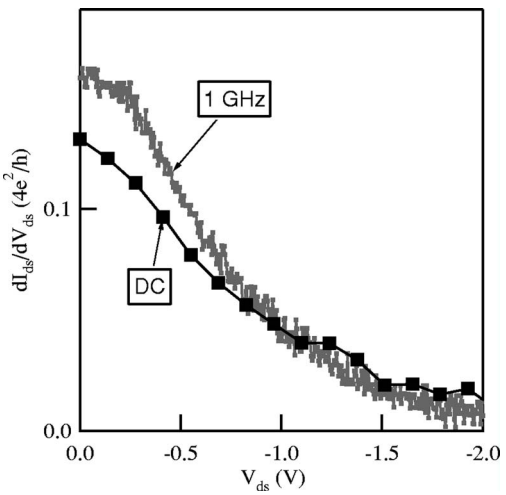

FIG. 4. Dynamical conductance at dc and 1 GHz at $V_{\text{gate}}=-8$ V.

trinsic cutoff frequency (i.e., the cutoff frequency in the absence of parasitics) is much larger than our measurement frequency of 1 GHz.

Although prior to this work SWCNT FET linear response has only been observed at megahertz frequencies,[10] recent work has demonstrated *rectification* in SWCNT FETs at frequencies up to 50 GHz.[11] This interesting and significant work provides quantitative information about device performance as a nonlinear rectifier (i.e., diode), and even gives information about the frequency limit of this nonlinearity. As nanodevices are predicted to be inherently fast,[1] it is a significant achievement to demonstrate the frequency dependence of this nonlinearity in order to experimentally prove the ultimate limits of nanodevices. However, rectification does not explicitly measure the small signal S matrix, especially its frequency dependence, and hence is a significant but somewhat indirect step towards ultrafast amplification of rf signals by a nanodevice. In addition, studies to date have focused on large signal rf voltages, so that the device is operating far out of the linear range. For applications such as amplifiers (both LNAs and power amplifiers), one is interested in *avoiding* nonlinearities. In particular, rectification does not address the frequency limitation of the gain of the device nor impedance matching requirements at the input and output. Both of these requirements are critical challenges that must be addressed head-on before any practical use is to be made of nanodevices of any kind in the rf and microwave frequency range.

For this reason, the measurement of the high bias dynamical source-drain conductance in a SWCNT FET presented herein is a significant step in that direction. Only when the entire 2×2 matrix has been measured will a rf characterization of SWCNT FETs be complete.

This work was supported by the U.S. Army Research Office (Award No. DAAD19-02-1-0387), the ONR (Award No. N00014-06-1-0268), and the National Science Foundation (Award Nos. ECS-0300557, CCF-0403582, and DMR-0216635).

[1] P. J. Burke, Solid-State Electron. **40**, 1981 (2004).
[2] Khairul Alam and Roger Lake, Appl. Phys. Lett. **87**, 073104 (2005); J. Guo, S. Hasan, A. Javey, G. Bosman, and M. Lundstrom, IEEE Trans. Nanotechnol. **4**, 715 (2005).
[3] G. Cuniberti, M. Sassetti, and B. Kramer, J. Phys.: Condens. Matter **8**, L21 (1996); Phys. Rev. B **57**, 1515 (1998); V. V. Ponomarenko, *ibid.* **54**, 10328 (1996); V. A. Sablikov and B. S. Shchamkhalova, JETP Lett. **66**, 41 (1997); V. A. Sablikov and B. S. Shchamkhalova, J. Low Temp. Phys. **118**, 485 (2000); V. A. Sablikov and B. S. Shchamkhalova, Phys. Rev. B **58**, 13847 (1998); M. Buttiker and T. Christensen, *Mesoscopic Electron Transport* (Kluwer, Dordrecht, 1997); M. Buttiker, H. Thomas, and A. Pretre, Phys. Lett. A **180**, 364 (1993); Y. M. Blanter, F. W. J. Hekking, and M. Buttiker, Phys. Rev. Lett. **81**, 1925 (1998); I. Safi and H. J. Schulz, Phys. Rev. B **52**, 17040 (1995); I. Safi, Eur. Phys. J. B **12**, 451 (1999); G. Y. Slepyan, S. A. Maksimenko, A. Lakhtakia, O. M. Yevtushenko, and A. V. Gusakov, Phys. Rev. B **57**, 9485 (1998); K. V. Pham, Eur. Phys. J. B **36**, 607 (2003).
[4] I. E. Aronov, N. N. Beletskii, G. P. Berman, D. K. Campbell, G. D. Doolen, and S. V. Dudiy, Phys. Rev. B **58**, 9894 (1998).
[5] William Liu, *Fundamentals of III-V Devices: HBTs, MESFETs, and HFETs/HEMTs* (Wiley, New York, 1999), xii.
[6] S. Li, Z. Yu, S. F. Yen, W. C. Tang, and P. J. Burke, Nano Lett. **4**, 753 (2004).
[7] Zhen Yu and Peter J. Burke, Nano Lett. **5**, 1403 (2005).
[8] Zhen Yu, Shengdong Li, and P. J. Burke, Chem. Mater. **16**, 3414 (2004); Shengdong Li, Zhen Yu, Christopher Rutherglen, and P. J. Burke, Nano Lett. **4**, 2003 (2004).
[9] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. J. Dai, Nature (London) **424**, 654 (2003).
[10] D. V. Singh, K. A. Jenkins, J. Appenzeller, D. Neumayer, A. Grill, and H. S. P. Wong, IEEE Trans. Nanotechnol. **3**, 383 (2004).
[11] J. Appenzeller and D. J. Frank, Appl. Phys. Lett. **84**, 1771 (2004); D. J. Frank and J. Appenzeller, IEEE Electron Device Lett. **25**, 34 (2004); Sami Rosenblatt, Hao Lin, Vera Sazonova, Sandip Tiwari, and Paul McEuen, Appl. Phys. Lett. **87**, 15311 (2005).