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AC performance of nanoelectronics: towards a ballistic THz nanotube transistor

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Abstract

We present phenomenological predictions for the cutoff frequency of carbon nanotube transistors. We also present predictions of the effects parasitic capacitances on AC nanotube transistor performance. The influence of quantum capacitance, kinetic inductance, and ballistic transport on the high-frequency properties of nanotube transistors is analyzed. We discuss the challenges of impedance matching for ac nano-electronics in general, and show how integrated nanosystems can solve this challenge. Our calculations show that carbon nano-electronics may be faster than conventional Si, SiGe, GaAs, or InP semiconductor technologies. We predict a cutoff frequency of 80 GHz/L, where L is the gate length in microns, opening up the possibility of a ballistic THz nanotube transistor.

1. Introduction

Nano-electronic devices fall into two classes: tunnel devices, and ballistic transport devices. In tunnel devices, single electron effects occur if the tunnel resistance is larger than $h/e^2 \approx 25$ kΩ. In ballistic devices with cross-sectional dimensions of order the quantum mechanical wavelength of electrons, the resistance is of order $h/e^2 \approx 25$ kΩ. At first glance, these high resistance values may seem to restrict the operational speed of nanoelectronics in general. However, the capacitance for these devices is also generally small, as is the typical source–drain spacing. This gives rise to very small RC times, and very short transit times, of order ps or less. Thus, the speed limit may be very large, up to the THz range.

In this paper we take a more careful look at the general arguments for the speed limits of nanoelectronic devices. We find that the coupling to the outside world will usually be slow or narrowband, but that the coupling to other nano-electronic devices can be extremely fast. A more concrete goal of this paper is to present models and performance predictions about the effects that set the speed limit in carbon nanotube transistors, which form an ideal test-bed for understanding the high-frequency properties of nano-electronics because they may behave as ideal ballistic 1d transistors.

2. Nanotube interconnects: quantum impedances

The first step towards understanding the high-frequency electronic properties of carbon nanotubes is to understand the passive, ac impedance of a 1d quantum system. We have recently proposed an effective circuit model for the ac impedance of a carbon nanotube [1,2]. While our model was formulated for metallic nanotubes, it should be approximately correct for semiconducting nanotubes as well. In the presence of a ground plane below the nanotube or top gate above the nanotube, there is electrostatic capacitance between the nanotube and the metal. Due to the quantum properties of 1d systems, however, there are two additional components to the ac impedance: the *quantum capacitance* and the

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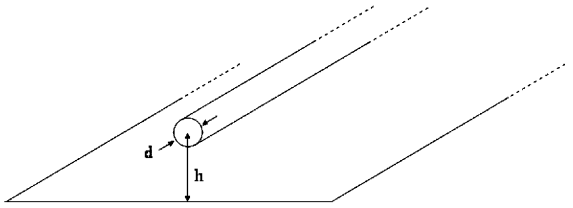

Fig. 1. Geometry for impedance calculations. The ground plane can be above or below the nanotube, corresponding to "top gate" or "back gate" devices.

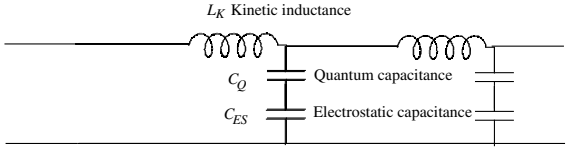

Fig. 2. Circuit diagram for a 1d nanowire or nanotube. Symbols are defined per unit length.

kinetic inductance. Thus, the equivalent circuit of a nanotube consists of three distributed circuit elements, which we summarize in Figs. 1 and 2.

2.1. Electrostatic capacitance

The electrostatic capacitance between a wire and a ground plane as shown in Fig. 1 is given by [3]

$$C_{\mathrm{ES}} = \frac{2\pi\varepsilon}{\cosh^{-1}(2h/d)} \approx \frac{2\pi\varepsilon}{\ln(h/d)}, \tag{1}$$

where the approximation is good to within 1% for $h > 2d$. (If the distance to the ground plane becomes larger than the tube length another formula for the capacitance has to be used, which involves replacing h with the length of the 1d wire.) For a typical value of h/d, this can be approximated numerically as

$$C_{\mathrm{ES}} \approx 50\ \mathrm{aF}/\mu\mathrm{m}. \tag{2}$$

2.2. Quantum capacitance

Because of the finite quantum energy level spacing of electrons in 1d, it costs energy to add an electron to the system. By equating this energy cost ΔE with an effective quantum capacitance e^2/C_{Q}, one arrives at the following expression for the (quantum) capacitance per unit length:

$$C_{\mathrm{Q}} = \frac{e^2}{\hbar\pi v_{\mathrm{F}}}, \tag{3}$$

where $\hbar$ is Planck's constant and v_{F} is the Fermi energy. The Fermi velocity for graphene and also carbon nanotubes is usually taken as $v_{\mathrm{F}} = 8 \times 10^5$ m/s, so that numerically,

$$C_{\mathrm{Q}} \approx 100\ \mathrm{aF}/\mu\mathrm{m}. \tag{4}$$

2.3. Kinetic inductance

Due to the inertia of electrons, the instantaneous velocity lags the instantaneous electric field in time. This means the current lags the phase, which can be described as a kinetic inductance. For 1d systems we have the following expression for the kinetic energy per unit length:

$$L_{\mathrm{K}} = \frac{\hbar\pi}{e^2 v_{\mathrm{F}}}. \tag{5}$$

Numerically,

$$L_{\mathrm{K}} = 16\ \mathrm{nH}/\mu\mathrm{m}. \tag{6}$$

In Ref. [1], we show that in 1d systems, the kinetic inductance will always dominate the magnetic inductance. This is an important point for engineering nanoelectronics: In engineering macroscopic circuits, long thin wires are usually considered to have relatively large (magnetic) inductances. This is not the case in nanowires, where the kinetic inductance dominates. This inductance can in principle be used as part of a tank circuit for on-chip, GHz passive signal processing components, currently under development [4,5].

2.4. Band structure, spin degeneracy

A carbon nanotube, because of its band structure, has two propagating channels [6]. In addition, the electrons can be spin up or spin down. Hence, there are four channels in the Landauer–Büttiker formalism. Taking this into account, in Ref. [1] we show that the circuit model of Fig. 1 is still valid as an effective circuit model for the charged mode if L_{K} is replaced by $L_{\mathrm{K}}/4$ and C_{Q} is replaced by $4C_{\mathrm{Q}}$.

Thus, the ac impedance of a nanotube consists of significant capacitive and inductive elements in addition to the real resistance which must be considered in any future nano-electronics system architecture.

3. Active devices: nanotube transistors

In this section, we extend our discussion to include active nanotube devices. A typical nanotube transistor geometry is shown in Fig. 3 below. In contrast to silicon transistors, the fundamental physical mechanism responsible for transistor action in nanotube transistors is still not completely understood. One action of the gate may be to modulate the (Schottky barrier) contact

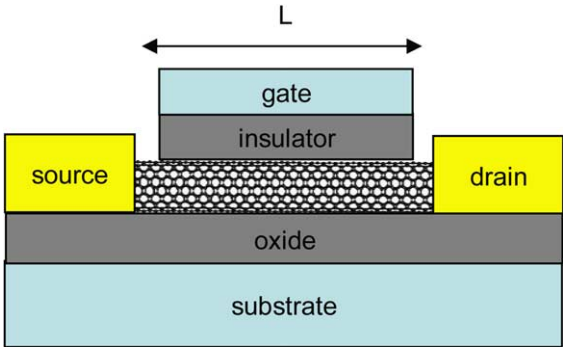

Fig. 3. Typical nanotube transistor geometry.

resistance [7]. Experiments also indicate that the source–drain voltage drops at least in part along the length of the nanotube [8], indicating that the contact is only one important element of the total source–drain resistance.

Complicating the issue is the question of whether the transport is diffusive or ballistic [9] (i.e. scatter free) from source to drain. Experiments [10] indicate that the mean free path in semiconducting nanotubes at room temperature is at least 1 μm, so that nanotubes shorter than 1 μm may behave as ballistic transistors. Rather than try to settle these issues, for the purposes of this paper, we will use experimentally measured parameters to predict device high-frequency performance.

4. Relevant frequency scales

We begin by estimating the frequency scales for the most important processes: the *RC* time and the transconductance.

4.1. RC time

The first important effect for high-frequency performance is the *RC* time. For a typical nanotube geometry of 0.1 μm length, *C* is of order 4 aF. *R* can be as small as 6.25 kΩ [6]. Therefore, the *RC* frequency is given by

$$\frac{1}{2\pi RC} \approx 6.3\ \text{THz} \tag{7}$$

This shows that the speed limit due to *RC* times intrinsic to a nanotube transistor is very large indeed.

4.2. Transconductance

The transconductance g_m over the gate–source capacitance C_{gs} sets another important frequency. Using an experimentally measured value [11] of 10 μS, this gives

$$\frac{g_m}{2\pi C_{gs}} \approx 400\ \text{GHz} \tag{8}$$

The above estimates indicate that a carbon nanotube transistor could be very fast, in spite of its high impedance. For more realistic estimates of device performance a small-signal equivalent circuit model would be very useful, especially for input and output impedance calculations and in order to investigate the effects of parasitic impedances on device performance.

5. Small-signal equivalent circuit

In this section, we propose a small-signal equivalent circuit model based on a combination of known physics in the small signal limit and generally common behavior for all field effect type devices. Our proposed active circuit model is not rigorously justified or derived. Rather, we hope to capture the essential physics of device operation and at the same time provide simple estimates of device performance.

We show in Fig. 4 our predicted small-signal circuit model for a nanotube transistor. In the following sections we discuss each of the important components.

5.1. Gate–source capacitance

The capacitance of a passive nanotube in the presence of a gate was discussed extensively in the first section; this can be used as an estimate of the gate–source capacitance C_{gs} in active mode; shown in Fig. 4. This capacitance includes the geometrical capacitance (50 aF/μm) in series with the quantum capacitance; the quantum capacitance is multiplied by 4 because of the band structure degeneracy. Thus:

$$\frac{1}{C_{gs}} \approx \frac{1}{C_{ES}} + \frac{1}{4C_Q} = \frac{1}{44\ \text{aF}/\mu\text{m}}. \tag{9}$$

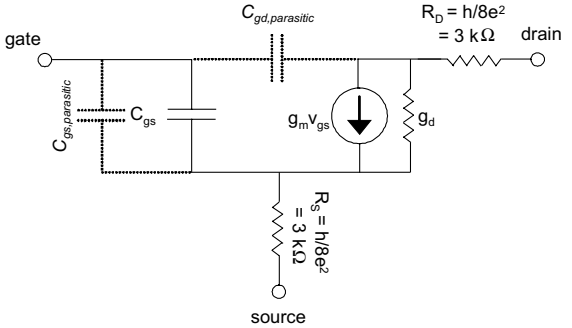

Fig. 4. Proposed small-signal circuit model for a nanotube transistor.

5.2. Transconductance

While the transconductance is the most critical parameter, the underlying mechanism is the least understood. In order to predict device high-frequency performance, we use experimental data from dc measurements as our guide. We show in Table 1 data from various research groups measured to date. Transconductances up to 20 μS have been measured [12], using an aqueous gate geometry. A transconductance of 60 μS was recently predicted [13,14] by simulation.

5.3. Drain resistance

In Fig. 4, g_d represents the output impedance of the device, if it does not appear as an ideal current source. In Table 1 (from Refs. [9,11–13,15–18]), we present some representative values from the literature which we have determined from the published source–drain I–V curves.

5.4. Series resistance

In most conventional transistors the series resistance consists of the metallization layer and the ohmic contact resistance. We argue that, in nanotube transistors, the intrinsic contact resistance will be of order the resistance quantum because of the 1d nature of the system. We elaborate.

At dc, the lowest value of resistance possible for a carbon nanotube is $h/4e^2$. This is because there are four channels for conductance in the Landauer–Büttiker formalism, each contributing h/e^2 to the conductance. To date very little experimental work has been done to measure the ac impedance of ballistic systems [19].

From a theoretical point of view, Büttiker and Christen [20] have carefully analyzed the case of a capacitive contact to a ballistic conductor (in his case a 2DEG without scattering) in contact with one dc electrical lead through a quantum point contact. They find that the ac impedance from gate to lead includes a real part, equal to half the resistance quantum $h/2e^2$. Based on this work we argue that a reasonable value for the contact resistance in our small-signal model would be $h/2e^2$ per channel. Since there are 4 channels in parallel, this gives a contact resistance of $h/8e^2$. There will be an additional imaginary contribution to the contact impedance (not shown) due to the kinetic inductance on the order of a few nH.

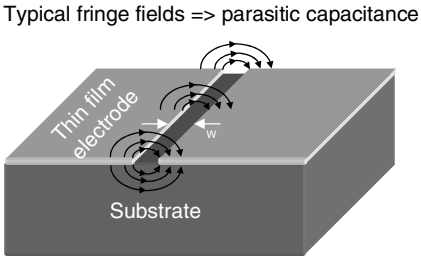

Fig. 5. Typical geometry giving rise to parasitic capacitance.

5.5. Parasitic capacitance

The parasitic capacitance is due to the fringing electric fields between the electrodes for the source, drain, and gate. While these parasitic capacitances are generally small, they may be comparable to the intrinsic device capacitances and hence must be considered.

There are no closed-form analytical predictions because the geometry of the electrodes will vary among different electrode designs. In order to estimate the order of magnitude of the parasitic capacitance, we can use known calculations for the capacitance between two thin metal films, spaced by a distance w, as drawn in Fig. 5. For this geometry, if w is 1 μm, the capacitance is $\sim 10^{-16}$ F/μm of electrode length [21]. For a length of 1 μm, this gives rise to $\sim 10^{-16}$ F. Thus, typical parasitic capacitances are of the same order of magnitude as typical intrinsic capacitances.

Table 1
Measured transconductance values taken from the literature [9,11–17] and the author's lab [18]

Ref.	T_{gate} (Å)	g_m (μs)	g_d (μs)	L (μm)	G_{on} ($4e^2/h$)
[15]	3000	0.3	0.03	0.1	0.006
[16]	1000	0.001	1	0.3	0.006
[17]	200	3	<0.1	1	0.017
[12]	0	20	<0.1	3	0.12
[11]	80	12	<0.1	1	0.06
[18]	500	0.05	0.6	10	
[13]*	10	60	<0.1	1	
[9]	5000	10	<0.1	0.3	0.5

The values of g_m, g_d, and G_{on} are calculated from the published I–V curves.
* Theory.

6. Cutoff frequency

In this section, we provide estimates of the cutoff frequency f_T, a standard yardstick for transistor high-speed performance, defined as the frequency at which the current gain falls to unity [22]. Based on the circuit model in Fig. 4, it can be shown [22] that f_T is given by:

$$\frac{1}{2\pi f_T} = (R_S + R_D)C_{gd,p} + \frac{1}{g_m}\left(C_{gs} + C_{gd,p} + C_{gd,p}\right) + \frac{g_d}{g_m}(R_S + R_D)\left(C_{gs} + C_{gd,p} + C_{gd,p}\right) \quad (10)$$

Here the p subscript denotes "parasitic". Using the experimentally measured transconductance of 10 μs, a parasitic capacitance value of 10^{-16} F, and a C_{gs} of 4×10^{-17} F (appropriate for a 1 μm long tube), we predict a cutoff frequency of 8 GHz. For this value, the parasitic capacitance is the most important contribution. Thus, minimizing the parasitic capacitance is of prime importance in increasing f_T for nanotube transistors.

6.1. Parasitic capacitance

While the above calculations show that the parasitic capacitance is important, in principle it should be possible to significantly reduce the parasitic capacitance by detailed electrode geometry design. Another (better) way to reduce the parasitic capacitance would be to use the nanotube itself as an interconnect electrode from one nanotube transistor to another. Then, the parasitic capacitance would be dramatically smaller than that with lithographically fabricated electrodes.

6.2. Scaling with gate length

If we assume the parasitic capacitances can be reduced to negligible values, Eq. (10) simplifies to

$$\frac{1}{2\pi f_T} = \frac{C_{gs}}{g_m} \quad (11)$$

C_{gs} scales linearly with gate length, and was calculated above. In the ballistic limit, g_m should be independent of gate length. Using the largest measured transconductance to date of 20 μs, this gives rise to the following prediction for f_T:

$$f_T = \frac{80\ \text{GHz}}{L_{gate}\ (\mu\text{m})} \quad (12)$$

We plot in Fig. 6 our predictions for f_T vs. gate length for a nanotube transistor, and compare to other technologies [23,24]. The predictions are very promising, suggesting that a nanotube transistor with THz cutoff frequencies should be possible.

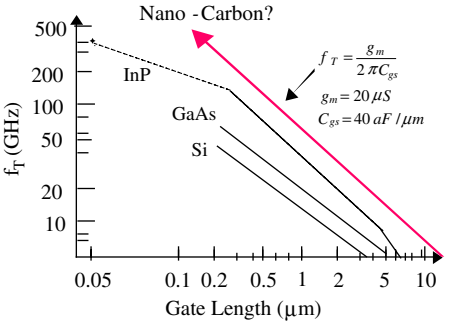

Fig. 6. f_T vs. gate length. References are: solid lines [23]; dashed line [24]; nano-carbon prediction: this work.

7. Noise performance: Towards the quantum limit?

One promising potential application is in low-noise analog microwave amplification circuits. Recent work on noise in mesoscopic systems has been extensive and has shown suppressed noise due to the Pauli exclusion principle [25]. Since electrons can travel without scattering from source to drain, and the Pauli exclusion principle suppresses the current noise, it may be possible to engineer extremely low noise microwave amplifiers using carbon nanotubes, possibly even approaching the quantum limit of sensitivity [26].

8. Challenges: impedance matching

Nano-devices generally have high resistance values, of order the resistance quantum $R_Q = h/e^2$. At high frequencies, for driving circuits more the one electromagnetic wavelength away from the device, the load impedance is typically of order the characteristic impedance of free space, $Z_C = (\mu\varepsilon)^{1/2} = 377\ \Omega$. The ratio of $Z_C/R_Q = 1/137$ has a special significance in physics and is called the fine structure constant; it is set by only three fundamental constants of nature: e, h, and c. For electrical engineering, this means that nano-devices will always need impedance matching circuits when driving loads more than a few cm away at rf and microwave frequencies.

Integration can provide a solution to this problem. For nano-electronic devices closely spaced, down to the nano-scale, the capacitive loading from one device to the next can be minimized. For full effect, the interconnects should be nano-scale as well; lithographically fabricated interconnects may be too large to realize the full potential of nano-electronics. Our work on the high-frequency electrical properties of active and passive nano-devices provides a very small step towards achieving this ultimate goal of *integrated nanosystems*.

9. Conclusions

In conclusion, we have presented phenomenological predictions for the ac performance of nanotube transistors. Based on our calculations, we predict carbon nanotube transistors may be faster than conventional semiconductor technologies. There are many challenges that must be overcome to meet this goal, which can be best be achieved by *integration* of nanosystems.

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