All-Semiconducting Nanotube Networks: Towards High Performance Printed Nanoelectronics

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ABSTRACT

In this work, we present progress towards devices fabrication using all semiconducting nanotubes as the starting material. Individual nanotubes are known to have intrinsic mobility of more than 10,000 cm²/V-s but using a network of nanotubes will decrease this mobility because of tube-tube screening effect and junction resistance. Here we are using solution-based deposition of purified 99% semiconducting single-walled nanotubes as the channel in field effect transistors. DC analysis of devices' characterization shows a high mobility, more than 50 cm²/V-s, and good on/off ratio in the range of more than 10^3 and 10^4 . A critical issue is the ink formulation and dependence of electronic properties on the nanotube density after deposition. In addition, the channel length also plays an important role in controlling both mobility and on/off ratio.

INTRODUCTION

So far different techniques have been utilized to fabricate carbon nanotube devices. To generally categorize these methods one can separate them in two major techniques, "depositing nanotubes" and "in-situ growth of nanotubes". Depositing nanotube from a solution has been investigated recently to find the best way of having sorted network of semiconducting nanotubes ¹⁻³. In addition to solution enrichment, semiconducting CNTs can be preferentially placed on wafers through modification of the wafer surface. It is now well known that amine terminated silanes such as 3-aminoprolyltriethoxysilane (APTES) when attached to the substrate surface, provide far better and selective deposition of nanotubes deposited from the solution and help the uniformity of the nanotube mat as well. For this study we combined both the processes, using semiconducting enriched solution of SWNTs and APTES assisted deposition of nanotubes. In this work, we present progress towards semiconducting nanotube field effect transistors using 99% semiconducting nanotubes as the starting material (this percentage is determined using spectroscopic methods such as Raman spectroscopy). Comparing to previous works ⁴⁻⁶ we are

getting higher mobility while using more semiconducting enriched nanotubes in our devices. Moreover, we study the effect of various gate lengths, which reveals an interesting trend between the channel length and the mobility. High mobility and very good on/off ratio was achieved showing a great improvement in the device characteristics.

EXPERIMENT

Devices reported here were fabricated using a solution enriched up to 99% in semiconducting single walled carbon nanotubes (diameter range - 1.2-1.7 nm, length range 300 nm to 5 µm). These solutions were made using density gradient centrifugation process for the separation of nanotubes with different chiralities. Prior to the deposition of nanotubes, the surface of Si/SiO₂ wafer was modified with APTES (a conventional method). Nanotube solution was then either spin-coated or poured on the wafers.

Following the nanotube deposition, the wafer was patterned for source and drain deposition using standard photolithography. We also studied the effect of gate length on mobility, and on/off ratio, for devices with different gate lengths ($20 \sim 100 \mu m$). E-beam evaporation was used to deposit source and drain electrodes (Pd/Au). The Si wafer acts as the back gate and 300 nm of SiO₂ was used as the gate dielectric.

The I_D - V_D extracted from the dc measurement shows that the current-voltage relationship is linear for small V_D ranging from -1 V to 1 V (triode region), indicating good ohmic contact between nanotubes and electrodes. By applying more negative V_D the devices clearly show saturation behavior. Since we are using purified all-semiconducting (99% semiconducting) tubes in the channel, we are expecting high on/off ratio, which is the case in our devices. The on/off ratio is more than 10000 in some devices. Mobilities more than 50 cm²/V-s are observed using conventional MOSFET equation (below) and curve fitting the I_D - V_D characteristic in the triode region.



Figure 1. **a**, Schematic diagram of the device with 300 nm thermally grown dry silicon-dioxide on top of a Si wafer and Pd/Au (15/30nm) source and drain electrodes for ohmic contact with random networks of the semiconducting nanotubes. **b**, SEM image of individual nanotube network deposited for the channel. **c**, Current-voltage characteristic of a device with channel length of 100 μ m and W = 200 μ m for different gate voltages ranging from +10 V to -10 V in 2 V steps, showing the expected saturation behavior at negative gate voltages and high drain-source voltage (V_{DS} changes from 0 V to 6 V).

$$\mu = \frac{L}{W} \frac{1}{C_{ox}} \frac{1}{V_{ds}} \frac{dI_{ds}}{V_{GS}}$$
(1)

Where, μ is the mobility, L and W are gate (channel) length and width respectively, C_{ox} is the oxide (dielectric) capacitance, V_{ds} and V_{GS} and I_{ds} are drain-source voltage, gate-source voltage and drain-source current respectively.

We have also investigated the relationship between the channel length variation and the mobility of the devices. Channel lengths from 20 μ m to 100 μ m have been studied. Figure 2 shows the trend between devices' mobility and their channel length. It is depicted that interestingly by increasing the channel length, the mobility will increase for 99% semiconducting tubes with a fixed tube density and fixed channel width (100 μ m).



Figure 2. Mobility vs. channel length for $L_{channel} = 20 \ \mu m$ to 100 μm . As a sample, the measurements were performed on devices with the moderate tube density of around 40 tubes per μm^2 and for 2 different semiconducting to metallic ratios in the solution. Tube density was controlled both by the surface modification and the density in the solution.

The density of the nanotubes in the channel is calculated using the SEM images and count the number of nanotubes in a $1x1 \mu m$ squares in different locations in the channel area. Also the deposited nanotube mat containes only 1 layer of nanotube almost in every locations. Because of using APTES, the samples look uniform all over the channel area however, there might be a

slight nonuniformity (less than $5\sim10\%$) that is assumed to be the source of scattering in the results shown in figure 2. The impact of the channel length on on/off ratio is currently under investigation.

CONCLUSIONS

In summary we reported thin film transistors fabricated using semiconductor-enriched carbon nanotubes. The dc electrical measurements show a great improvement in terms of mobility (more than 50 cm²/V-s) and on/off ratio (more than 10000), compared to previous works. Moreover, it has been shown that by increasing the channel length, the mobility will also increase for purified semiconducting nanotube-network transistors. Since these are some of the first spin-on, all semiconducting nanotube devices ever made, these initial results are indeed quite promising for printed electronics.

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