# Aligned Array FETs as a Route Towards THz Nanotube Transistors

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**ABSTRACT**

The development of nanowire and nanotube FETs for high frequency applications faces a challenge of impedance matching, due to the inherent mismatch between the resistance quantum (≈ 25 kΩ) typical of nanodevices, and the characteristic impedance of free space (≈ 377 Ω) typical of RF circuits. One possible solution is to use parallel nanotube or nanowire FETs to decrease the input impedance, and increase the drive current. In this paper, we present our progress towards this goal using aligned arrays of nanotube FETs. Initial studies on randomly oriented CVD grown devices give mobilities of 4 $cm^2$/V-s. These initial devices carry ≈ 0.25 mA of current. Even higher mobilities (hence very high operational frequencies up to THz) should be possible with aligned nanotube FETs.
**Keywords:** Nanotube, nanowire, nanotechnology, GHz, THz.

## 1. INTRODUCTION

The development of single-walled nanotube (SWNT) electronics[1] has been motivated by the fact that nanotubes can function as very small diameter wires, of order a few nm, which is beyond the size that can be fabricated by any current or projected lithographic method. This has allowed for studies of device physics in the nano regime, as well as possible technological applications. Much has been learned, and there are clearly some advantages of nanotube FETs to be seriously considered as an alternative to scaled Si CMOS beyond "The Roadmap"[2].

One potential advantage of nanotube FETs is that, in principle, they can be very high speed (up to THz)[3]. A challenge for *integration* into circuits, which we discuss in more depth below, is the high impedance and low current capability of SWNT FETs. In this conference paper, we describe our recent progress towards one possible solution to this challenge: parallel arrays of nanotube FETs. Recent work in our labs[4, 5] and at Duke[6-10] on the synthesis and electrical characterization of ultra-long (many mm), well-aligned, 1d arrays of SWNTs provides the technological basis for the beginnings of such a study. By fabricating aligned SWNT array FETs, the promise of THz frequency nanotube transistors may eventually be realized.

## 2. INDIVIDUAL SNWT FETS: BACKGROUND

### 2.1. Individual SWNT FETs: DC performance

#### 2.1.1. Typical geometry

Individual SWNTs can be either semiconducting or metallic, depending on their chirality. At the moment, there is no way to control which kind are synthesized on an individual nanotube basis. Semiconducting nanotubes have a bandgap that is approximately 1 eV/d[nm], where d is the diameter. These semiconducting nanotubes can be gated on and off, in a geometry that is typically of the form shown in Fig. 1.

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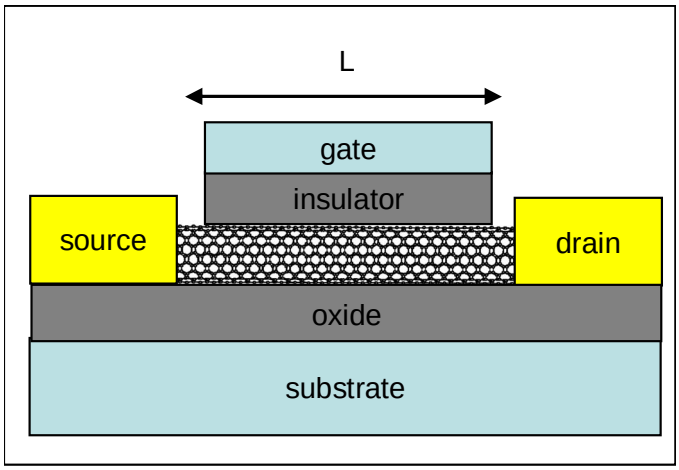


**Fig. 1:** Typical individual SWNT FET geometry.

Referring to Fig. 1, the source/drain electrodes are typically formed by evaporating metal onto the top of the nanotube after it is deposited onto a solid substrate, such as oxidized Si. In initial studies, the substrate was used as the gate. However, in order to allow individual addressing of SWNT FETs on a wafer, and in order to reduce source-gate capacitance (important for high-speed), top-gates can be deposited if a suitable dielectric can be found which does not damage the SWNT[11-13].

### 2.1.2. Lowest "ON" resistance is 6 kΩ

According to the Landauer-Buttiker theory of conductance in quantum confined geometries (such as a SWNT), the lowest value of resistance for a ballistic, one-channel conductor (with perfect, adiabatic contacts) at dc is given by $h/e^2 \approx$ 25 kΩ. In a SWNT, there are four effective channels, so that the lowest dc resistance is given by $h/4e^2 \approx 6$ kΩ. Thus, in practical terms, the lowest resistance possible for a SWNT FET, with "perfect" electrical contacts, and ballistic (scatter-free) transport from source to drain, is 6 kΩ. This can be thought of as a "contact resistance". Compared to Si CMOS, this is quite a large resistance and will be a challenge to implement in integrated circuits. To be clear, this contact resistance cannot be reduced by clever fabrication techniques; it is inherent in quantum mechanics. *According to quantum mechanics, the lowest "on" resistance for a SWNT FET is 6 kΩ.*.

In terms of current-carrying capacity, this translates into about 10 μA of current carried by each SWNT FET. This is simply because the S-D voltage is typically of order 1 V, and the contact resistance is not always as low as 6 kΩ. Currents up to 100 μA through a SWNT FET have been reported in the literature[14].

It should be noted that achieving this theoretical limit from a practical point of view is not trivial, and special attention must be paid to the contact between the nanotube and the source/drain electrode. Recently, this theoretical limit on the dc resistance was achieved in SWNT FETs experimentally[15].

### 2.1.3. Mechanism of transistor action: Contact resistance modulation of bulk charge modulation?

For short nanotubes, the mechanism of transistor action is generally believed to be due to the modulation of the contact resistance at the boundary of the metal/nanotube system, which forms a Schottky barrier. This Schottky barrier, if it is large, prevents the "on" resistance from approaching the 6 kΩ limit[16]. As mentioned above, Javey[15] has recently developed contact technology to significantly suppress the Schottky barrier contact resistance, so that the mechanism of transistor action in those devices is more complicated. Durkop[17] recently studied 300 μm long nanotubes, and concludes that they are classical field effect transistors, i.e. that the contact resistance is not the dominant part of the nanotube resistance. Additionally, Durkop found a field-effect mobility of 200,000 $cm^2$/V-s, higher than any other material known to man. This was followed by our recent work on SWNT FETs an order of magnitude longer, 0.4 cm, which came to similar conclusions[5]. It is clear that the contact resistance, as well as the resistance due to scattering along the

nanotube, can be significant, depending on the geometry involved. A quantitative theoretical statement of this qualitative conclusion would be a useful development.

### 2.2. Individual SWNT FETs: AC performance

In contrast to work on the dc performance of SWNT FETs, the ac performance is only now beginning to be studied. The system is more complicated because of capacitive and inductive effects. Even for a simple metallic nanotube without a gate, the effective ac circuit is complicated and the impedance is not restricted by $h/e^2$, although it is typically of that order[18, 19]. We recently demonstrated[20] the operation of carbon nanotube transistors at a spot microwave frequency (2.6 GHz) at cryogenic temperatures; room temperature and swept-frequency experiments to more quantitatively characterize the high frequency properties of individual SWNT FETs are currently underway in our labs.

In the absence of rigorous theoretical models, we recently developed a phenomenological model[3] for the ac performance of SWNT FETs. There, we concluded that if the parasitic capacitance is neglected, the intrinsic speed limit of a SWNT FET could be of order THz. However, the output impedance in our simple model is typically of order 6 kΩ, and any realistic parasitic capacitance at either the input or the output prevents the intrinsic speed limit of SWNT FETs from being achieved. This is one of our motivations for investigating AC performance of SWNT array FETs.

## 3. SNWT ARAY FETS

In this section we review prior work on randomly oriented arrays of SWNTs as FETs, and then present our goal of *aligned* SWNT array FETs. At the moment, we do not have a circuit model for the ac performance of either of these FETs. However, the mobilities determined through transport measurements are quite good; these, combined with the high current carrying capacity (and hence low resistance) of SWNT array FETs makes them very promising for high-frequency applications. In particular, this may be a way to approach the intrinsic speed limit of SWNT FETs, which can be in the THz range.

### 3.1. Background: random network SWNT FETs

SWNTs can be synthesized in bulk by laser ablation and spin-coated onto any substrate to attain randomly oriented mats. E. Snow has shown that these can be contacted electrically and used to make SWNT array FETs[21]. These can even be deposited on polymeric substrates[22]. Snow found a mobility as high as 50 $cm^2$/V-s. This is probably due to the intrinsic high mobility of SWNTs. In Snow's studies, the spacing between electrodes was probably less than the average nanotube length, so that on average not all nanotubes were in electrical contact with both electrodes. Given this, the mobility measured is quite good.

### 3.2. Towards aligned SWNT array FETs

Our ultimate goal in this work is to use recently developed techniques[4-10] to synthesize aligned arrays of ultra-long (~ mm) SWNT nanotubes and incorporate them into array FETs. Since every single nanotube would be in contact with the source and drain electrodes, the mobility and current carrying capacity should be quite high. This is indicated schematically in Fig. 2.

### 3.3. This work: Experimental progress

In this work, we present measurements on chemical vapor deposition (CVD) grown SWNT array FETs. While our preliminary studies are on randomly oriented SNWT arrays, the significance of these studies is two-fold: First, we find a mobility of 4 $cm^2$/V-s. Second, we present CVD techniques to synthesize aligned arrays of ultra-long SWNTs, and our designs for synthesizing aligned SWNT array FETs from these.

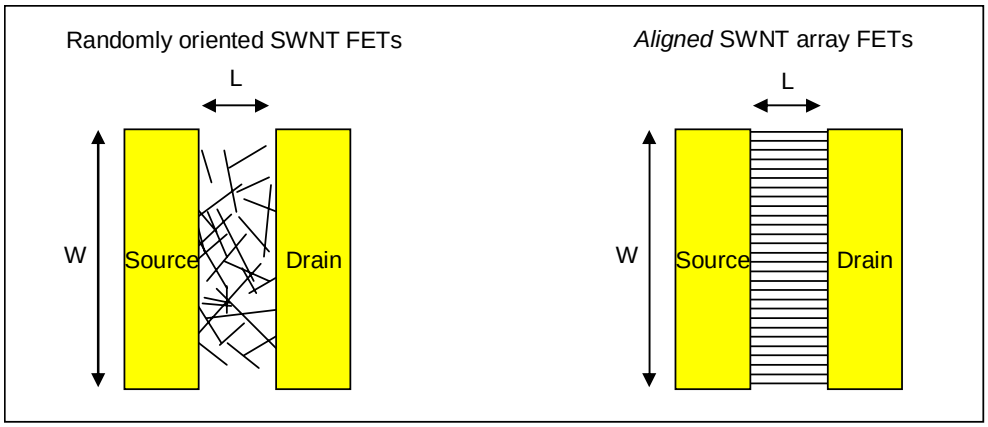


**Fig. 2:** Schematic diagram of random and aligned SWNT array FETs.

## 4. SYNTHESIS AND DEVICE FABRICATION

### 4.1. CVD synthesis of randomly oriented mats

For the pre-growth catalyst preparation, we started with a 4-inch Si wafer (100, p-type, resistivity 12-16 kΩ-cm) with a 500 nm thick $SiO_2$ film as a substrate. An aqueous suspension of Fe laden alumina nanoparticle catalysts was applied uniformly and allowed to dry in air. The nanoparticle suspension was prepared by adding 0.3 g of alumina nanoparticles (Degussa, aluminum oxide C), 0.05 mmol of $Fe(NO_3)_3 \cdot 9H_2O$ (Aldrich), and 0.015 mmol of $MoO_2(acac)_2$ (Aldrich) to 300 ml DI water (18 MΩ-cm). The mixture was stirred for 24 hours and sonicated for 1 hour.

The synthesis was carried out using a home-built CVD system based on a 3 inch diameter Lindberg furnace, with a specially designed gas-flow injector to minimize turbulent flow. The growth procedure was as follows: First, the sample was heated to 900 C in Ar over the course of 1.5 hours. Next, $H_2$ was flowed for 10 minutes. Next, a methane (1000 sccm)/$H_2$ (200 sccm) mixture was flowed for 15 minutes to activate the growth. The sample was then allowed to slowly cool in Ar. Post-growth characterization was carried out with SEM (S-4700-2 FESEM, Hitachi, Japan) and AFM (Digital Instruments, Multimode).

### 4.2. Device fabrication of randomly oriented mats

The mats were located with respect to predefined alignment marks via SEM. Devices were fabricated by evaporating a Pd(20 nm)/Cr(20 nm)/Au(100 nm) tri-layer onto the randomly oriented mats and lifting off in acetone. Electron-beam lithography was used to define the source-drain electrode spacing of 2 μm. The gate width was 100 μm. For these initial studies, the nanotubes away from the electrodes (i.e. outside of the region between the source-drain gap) were not removed (Fig. 3).

### 4.3. Synthesis and device fabrication of aligned SWNT arrays

For the pre-growth catalyst preparation, we started with a 4-inch Si wafer (100, p-type, resistivity 12-16 kΩ-cm) with a 500 nm thick $SiO_2$ film as a substrate. A thin Cr/Au (50 nm/200nm) bilayer was deposited by e-beam or thermal evaporation and patterned with photo-lithographically using liftoff. After definition of the metallization pattern, photoresist was applied, exposed, and developed, to fabricate wells in the resist over the Cr/Au pattern. An aqueous suspension of Fe laden alumina nanoparticle catalysts was applied and allowed to dry in air, then lifted off in acetone. The result is a lithographically defined Cr/Au/nanoparticle catalyst pattern ready for growth. The nanoparticle suspension was prepared as for the randomly oriented mats. The CVD synthesis recipe was carried out as for the randomly oriented mats. Devices will be fabricated as in the randomly oriented case, using Pd/Cr/Au electrodes (Fig. 4).

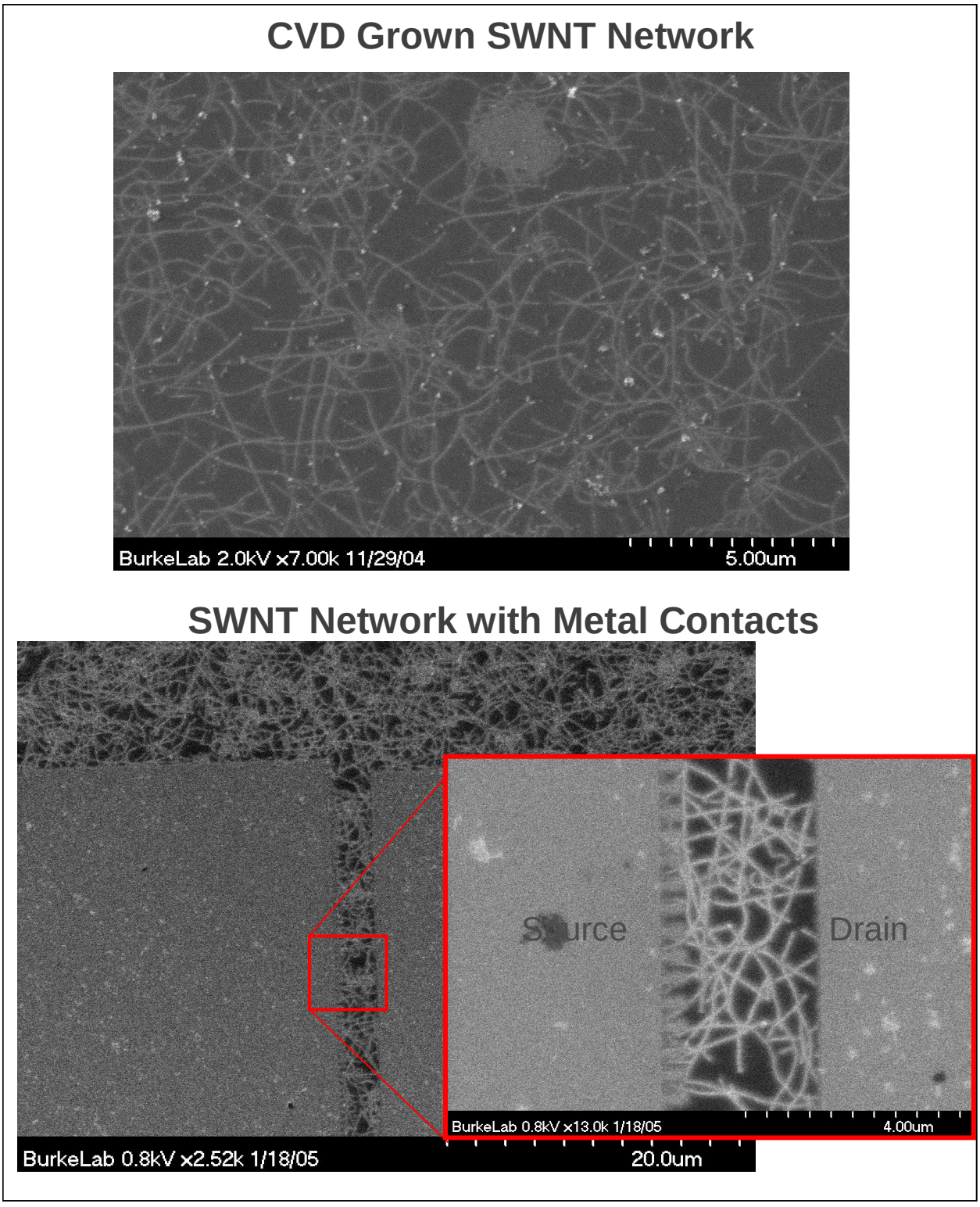


**Fig. 3:** Randomly oriented SWNT network FET.

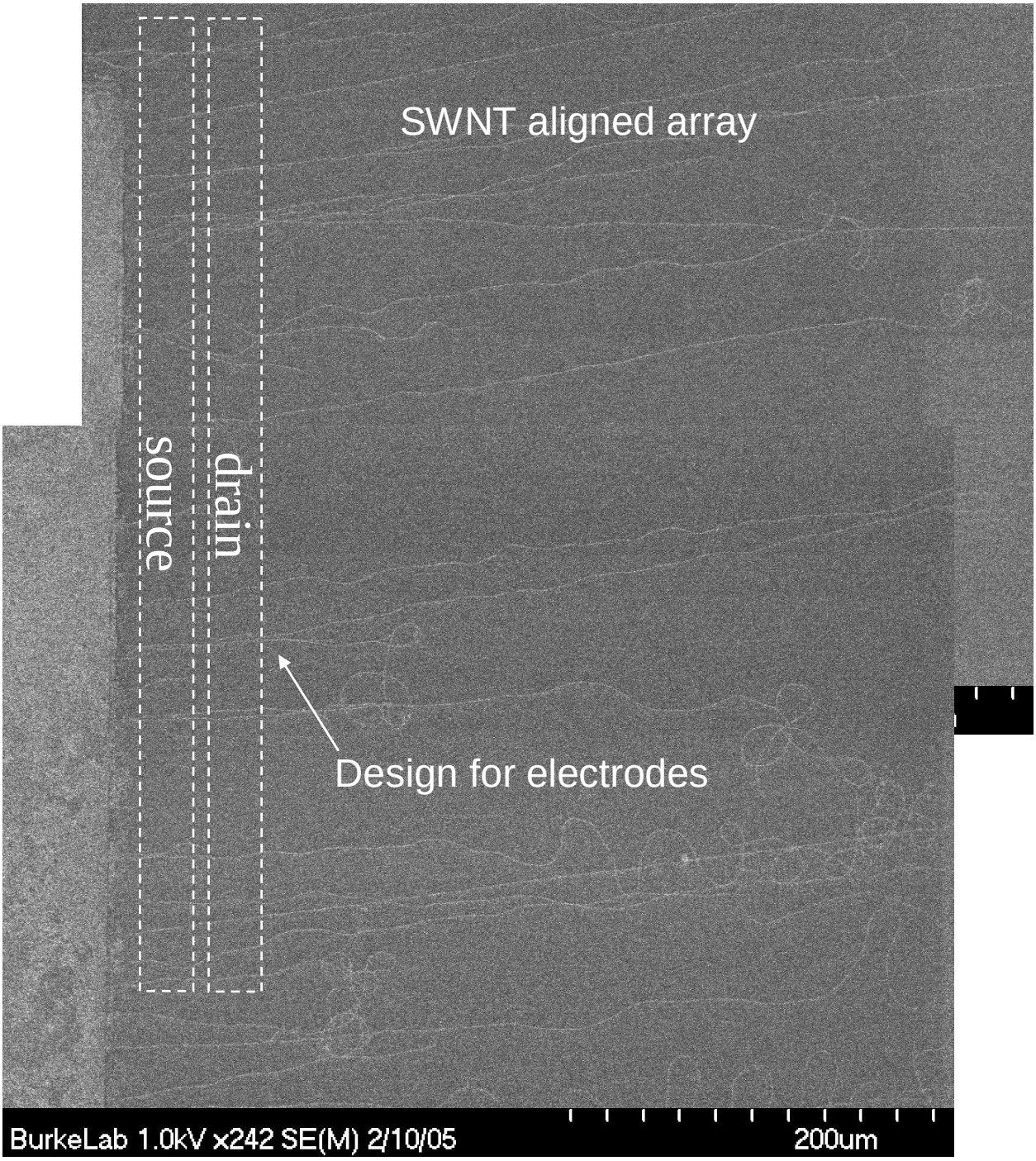


**Fig. 4:** Aligned array FET based on long nanotubes.

## 5. DEVICE PERFORMANCE OF RANDOMLY ORIENTED SWNT FET

Fig. 5 shows the measured I-V curves and depletion curves of one of the devices. The data show that the devices are able to carry up to ≈ 0.25 mA of current. The on/off ratio is only about 5; this may be due to the presence of metallic nanotubes within the gap, as well as nanotube away from the gap which are not gated as efficiently. From the low bias depletion curve, we can estimate the field-effect mobility using the standard formula:

$$\mu_{eff} \equiv \frac{(dI/dV_g)L_{ox}L_{sd}}{\varepsilon W_{sd}V_{sd}} = \frac{26nA/V * 500nm * 2\mu m}{3.9 * 8.85 * 10^{-12} F/m * 100\mu m * 20mV} = 4cm^2/Vs, \quad (1)$$

where $\mu_{eff}$ is the effective field-effect mobility, $dI/dV_g$ the transconductance, $L_{ox}$ the thickness of the gate oxide, $L_{sd}$: the channel length, $\varepsilon$ the dielectric constant of the gate oxide, $W_{sd}$: the channel width, $V_{sd}$ the source drain voltage, and where we have inserted our parameters for this experiment. Our next step will be to measure the mobility on aligned SWNT array FETs.

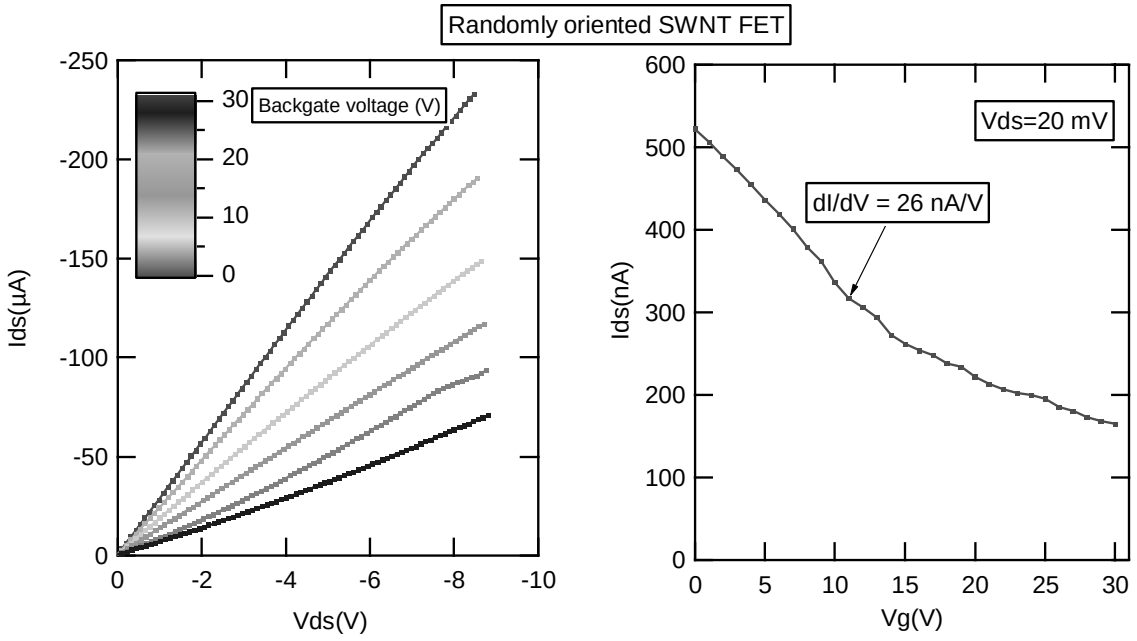


**Fig. 5:** Electrical properties of random mat SWNT FETs.

## 6. CONCLUSIONS

We have taken the first steps on the route towards aligned SWNT array FETs. Our preliminary results on randomly oriented SWNT FETs gave a promising mobility of 4 $cm^2$/V-s. In the future, we anticipate that the aligned SWNT array FETs will give much higher mobility. While much work is left to be done, the array approach should allow for low output impedance and low input impedance. Coupled with the high intrinsic speed limit of SWNT FETs, these array devices should be able to achieve THz cutoff frequencies.

## 7. ACKNOWLEDGEMENTS

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