UNIVERSITY OF CALIFORNIA,
IRVINE

Carbon Based Transistors and Nanoelectronic Devices

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical and Computer Engineering

by

Nima Rouhi

Dissertation Committee:
Professor Peter John Burke, Chair
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2011

DEDICATION

To

my beloved Faezeh, and my parents, Rouhollah and Afsaneh

Table of Contents

List of Figures

List of Tables

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  Electrical Engineering and Computer Science Department

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  Fabrication and analysis of nanoelectronic devices based on ***Carbon Nanotube*** for *high mobility, high on/off ratio,* and *high frequency* field-effect transistors

  Fabrication and analysis of FETs and Sensors using mono/few-layer ***Graphene*** membrane

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- **A-Z Nanotechnology:**
  http://www.azonano.com/news.aspx?newsID=22878
- **Crazy Engineers:**
  http://www.crazyengineers.com/california-university-students-find-speed-of-tangled-transistor-547/

Publications

JOURNALS:

[9] **N. Rouhi**, *et al*, *"Broadband sheet conductivity of single and multilayer Graphene: DC to THz", in preparation*, 2011.

[8] **N. Rouhi**, *et al*, *"Electrolyte-gated single and multi-layer suspended graphene membrane", in preparation*, 2011.

[7] **N. Rouhi**, D. Jain, P. J. Burke, *"High-Performance Semiconducting Nanotube Inks: Progress and Prospects",* ACS Nano, *published online Oct 4th*, DOI: 10.1021/nn201828y, 2011.

[6] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *"Fundamental Limits on the Mobility of Nanotube-Based Semiconducting Inks"*, Advanced Materials, *Vol. 23, issue 1, pp. 94-99*, (Online Oct. 2010) Jan 2011.
(Also highlighted in ***IEEE Spectrum***, ***A-Z Nano***, ***Crazy Engineers***: http://spectrum.ieee.org/tech-talk/semiconductors/nanotechnology/tangled-nanotubes-make-speedy-transistors)

[5] D. Jain, **N. Rouhi**, and P. J. Burke, *"Electronics of nanotube arrays based on their deposition process*", Journal of Nanoscience and Nanotechnology, in press, 2011.

[4] D. Jain, **N. Rouhi**, C. Rutherglen, C. Densmore, S. Doorn and P. J. Burke, *"Effect of source, surfactant, and deposition process on electronic properties of carbon nanotube arrays",* Journal of Nanomaterials, *Vol. 2011, Article ID 174268*, DOI:10.1155/2011/174268, 2011.

[3] **N. Rouhi**, D. Jain, P. J. Burke, *"Nanoscale Devices for Large-Scale Applications"*, IEEE Microwave Magazine, *Vol. 11, issue 7, pp. 72-80*, 2010.

[2] S. Kang, C. Rutherglen, **N. Rouhi**, P.J. Burke, L.N. Pfeiffer, K.W. West, *"RF Circuit Model of a Quantum Point Contact"*, IEEE Sensors Journal, *Vol. 10, No. 3, pp. 391-394,* 2010.

[1] **N. Rouhi**, B. Esfandyarpour, S. Mohajerzadeh, P. Hashemi, M. D. Robertson, K. Raffel, *"Low temperature growth of silicon dioxide using hydrogenation assisted nano-crystallization and plasma enhanced oxidation"*, Journal of Non-Crystalline Solids (Elsevier), *Vol. 356, pp. 1027-1031*, 2010.

CONFERENCES (Peer-Reviewed):

[21] **N. Rouhi**, P. J. Burke, *"CNT RF Nanotechnology"*, IEEE Radio Wireless Week (RWW) 2012 (SiRF 2012), *Jan. 2012*, Santa Clara, CA, USA. (Invited)

[20] **N. Rouhi**, D. Jain, S. Capdevila, L. Jofre, E. Brown, P. J. Burke, *"Sheet Resistance of Multi-Layer Graphene in Radio Frequency"*, NANO DDS 2011, *Aug. 2011*, Brooklyn, NY, USA.

[19] **N. Rouhi**, D. Jain, S. Capdevila, L. Jofre, E. Brown, P. J. Burke, *"Broadband Conductivity of Graphene from DC to THz"*, IEEE NANO 2011, *Aug. 2011*, Portland, CA, USA. (Invited)

[18] D. Jain, **N. Rouhi**, P. J. Burke, *"Novel Approach Towards Performance Enhancement of All Semiconducting Carbon Nanotube Devices for Printed Electronics"*, IEEE NANO 2011, *Aug. 2011*, Portland, CA, USA. (Invited)

[17] **N. Rouhi**, D. Jain, P. J. Burke, *"Carbon Nanotube Purified Ink-Based Printed Thin Film Transistors: Novel Approach in Controlling the Electrical Performance"*, DRC (Device Research Conference) 2011, *June 2011*, Santa Barbara, CA, USA.

[16] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *"Performance Control of High Mobility, Printed Thin Film Transistors Using Semiconducting Nanotube Ink"*, MRS Spring meeting 2011, *April 2011*, San Francisco, CA, USA.

[15] D. Jain, **N. Rouhi**, K. Zand, P. J. Burke, *"All-Semiconducting nanotube networks Thin Film Transistors: An Insight Towards High Performance Printed Nanoelectronics"*, APS March meeting 2010, *March 2011*, Dallas, TX, USA.

[14] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *"All-semiconducting Nanotube Networks: Towards High Performance Printed Nanoelectronics"*, MRS Fall meeting 2010, *November 2010*, Boston, MA, USA.

[13] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *"Semiconducting-Enriched Printed Carbon Nanotube Mat used for Fabrication of Thin Film Transistors"*, IEEE NANO 2010, *August 2010*, Korea.

[12] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *" Semiconductor-Enriched Carbon Nanotube Thin Film Transistors"*, International Symposium on Spectral Sensing Research (ISSSR 2010), *June 2010*, Springfield, MO, USA.

[11] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *"Carbon Nanotube Field Effect Transistors using Printed Semiconducting Tubes"*, NSTI-Nanotech 2010, *June 2010*, Anaheim, CA, USA.

[10] D. Jain, **N. Rouhi**, C. Rutherglen, P. J. Burke, *"Effect of source, surfactant, and deposition process on electronic properties of carbon nanotube arrays"*, NSTI-Nanotech 2010, *June 2010*, Anaheim, CA, USA.

[9] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *"All-semiconducting nanotube devices for RF and microwave applications"*, IEEE MTT International Microwave Symposium (IMS 2010), *May 2010*, Anaheim, CA, USA. (Invited)

[8] D. Jain, **N. Rouhi**, C. Rutherglen, P. J. Burke, *"Effect of source, surfactant, and deposition process on electronic properties of nanotube arrays"*, NanoDDS-09, *Sept. 2009*, Fort Lauderdale, FL, USA.

[7] H. Zareie, N. Davoudzadeh, J. Koohsorkhi, S. Mohajerzadeh, **N. Rouhi**, "*New carbon nanotube antenna simulation and fabrication*", SPIE, *March 2009*, San Diego, CA, USA.

[6] P.J. Burke, C. Rutherglen, **N. Rouhi**, "THz Spectral Sensing with Nanotechnology: An Overview", International Symposium on Spectral Sensing Research (ISSSR 2008), *June 2008*, Hoboken, NJ, USA.

[5] S. Kang, C. Rutherglen, **N. Rouhi**, P. J. Burke, L.N. Pfeiffer, K.W. West, *"RF Circuit Model of a Quantum Point Contact"*, International Symposium on Spectral Sensing Research (ISSSR 2008), *June 2008*, Hoboken, NJ, USA.

[4] **N. Rouhi**, B. Esfandyarpour, S. Mohajerzadeh, P. Hashemi, B. Hekmatshoar, and M.D. Robertson, *"Low Temperature High Quality Growth of Silicon-Dioxide Using Oxygenation of Hydrogenation-Assisted Nano-Structured Silicon thin Films"***,** MRS Spring meeting 2007, *April 2007*, San Francisco, CA, USA.

[3] J. Koohsorkhi, **N. Rouhi**, Y. Abdi, S. Mohajerzadeh, M.D. Robertson and R.D. Thompson, *"Fabrication and Modeling of CNT Field-Emission Devices"***,** NSTI-Nanotech 2007, *May 2007*, Santa Clara, CA, USA.

[2] J. Koohsorkhi, **N. Rouhi**, S. Mohajerzadeh, M.D. Robertson, *"Fabrication and Modeling of Carbon Nanotube-Based Field Emission Devices"*, ElectroChemical Society (ECS) 2007, *October 2007*, Washington, DC, USA.

[1] M. Esfahani, S. Mohajerzadeh, A.Goodarzi, **N. Rouhi**, R.S. Tarighat, *"Laterally Encapsulated Cathode Structure for DC Plasma Display Panels (PDPs)"*, SID (Society for Information Display)-IMID (International Meeting on Information Display), 2005, Korea.

CONFERENCES (Invited Talks / Presentations):

[9] **N. Rouhi**, Dheeraj Jain, P. J. Burke, *"Novel Approach Towards Performance Enhancement of All Semiconducting Carbon Nanotube Devices for Printed Electronics"*, IEEE Nano 2011, *August 2011*, Portland, OR, U.S.A.

[8] **N. Rouhi**, D. Jain, P. J. Burke, *"Carbon Nanotube Purified Ink-Based Printed Thin Film Transistors: Novel Approach in Controlling the Electrical Performance"*, DRC (Device Research Conference) 2011, *June 2011*, Santa Barbara, CA, USA.

[7] **N. Rouhi**, P. J. Burke, *"Printed Nanoelectronics for RF and Microwave applications"*, IEEE MTT-IMS 2011, *June 2011*, Baltimore, MD, U.S.A.

[6] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *"Performance Control of High Mobility, Printed Thin Film Transistors Using Semiconducting Nanotube Ink"*, MRS Spring meeting 2011, *April 2011*, San Francisco, CA, USA.

[5] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *"All-semiconducting Nanotube Networks: Towards High Performance Printed Nanoelectronics"*, MRS Fall meeting 2010, *November 2010*, Boston, MA, USA.

[4] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *"Carbon Nanotube Field Effect Transistors using Printed Semiconducting Tubes"*, NSTI-Nanotech 2010, *June 2010*, Anaheim, CA, USA.

[3] **N. Rouhi**, D. Jain, K. Zand, P. J. Burke, *"All-semiconducting nanotube devices for RF and microwave applications"*, IEEE MTT International Microwave Symposium (IMS 2010), *May 2010*, Anaheim, CA, USA. (Invited)

[2] D. Jain, **N. Rouhi**, C. Rutherglen, P. J. Burke, *"Effect of source, surfactant, and deposition process on electronic properties of nanotube arrays"*, NanoDDS-09, *Sept. 2009*, Fort Lauderdale, FL, USA.

[1] H. Zareie, N. Davoudzadeh, J. Koohsorkhi, S. Mohajerzadeh, **N. Rouhi**, "*New carbon nanotube antenna simulation and fabrication*", SPIE, *March 2009*, San Diego, CA, USA.

Honors and Awards

- **Ph.D. Dissertation Award (Ranked 1st in EECS department)** *2011*
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- **APSIH-FRF Award** (Award of Excellence in Engineering) *2011*
- **APSIH Award** (Iranian-American Ph.D. Graduates Award) *2011*
- **IEEE Orange County "*Student Design Contest Award*"** *2010*
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- **IEEE Orange County "*Student Design Contest Award*"** *2008*
  6th International SoC Conference, sponsored by ***Western Digital Corporation***
- **Graduate Student Researcher Fellowship**, University of California-Irvine *2007 - 2008*
- **M.Sc. Thesis Award** *2007*
  "Iranian Presidential Award of the year" by the "Iranian Nanotechnology Initiative Council"
- **Nationwide Universities Entrance Exam Ranking - (Konkoor)** *2001*
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- **Top 10 Students – *"Exceptional Talents"* Award,** Univ. of Tehran *2001*
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Professional / Educational Activities

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- Official Reviewer of "Advanced Materials"
- Official Reviewer of "Advanced Functional Materials"
- Official Reviewer of "Applied Physics Letters"
- Official Reviewer of "IEEE Transactions on Nanotechnology"
- Official Reviewer of "Optics Express"
- Official Reviewer of "IEEE Transactions on Microwave Theory and Techniques"
- Program Committee member of "*IEEE ISDRS 2011*" Conference *2011*
- Official Reviewer of "*MRS Fall Meeting 2011*" Conference *2011*
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ABSTRACT OF THE DISSERTATION

Carbon Based Transistors and Nanoelectronic Devices

By

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Doctor of Philosophy in Electrical and Computer Engineering

University of California, Irvine, 2011

Professor Peter Burke, Chair

Carbon based materials (carbon nanotube and graphene) has been extensively researched during the past decade as one of the promising materials to be used in high performance device technology. In long term it is thought that they may replace digital and/or analog electronic devices, due to their size, near-ballistic transport, and high stability. However, a more realistic point of insertion into market may be the printed nanoelectronic circuits and sensors. These applications include printed circuits for flexible electronics and displays, large-scale bendable electrical contacts, bio-membranes and bio sensors, RFID tags, etc. In order to obtain high performance thin film transistors (as the basic building block of electronic circuits) one should be able to manufacture dense arrays of all semiconducting nanotubes. Besides, graphene synthesize and transfer technology is in its infancy and there is plenty of room to improve the current techniques. To realize the performance of nanotube and graphene films in such systems, we need to economically fabricate large-scale devices based on these materials. Following that the performance control over such devices should also be considered for future design variations for broad range of applications.

Here we have first investigated carbon nanotube ink as the base material for our devices. The primary ink used consisted of both metallic and semiconducting nanotubes which resulted in

networks suitable for moderate-resistivity electrical connections (such as interconnects) and rf-matching circuits. Next, purified all-semiconducting nanotube ink was used to fabricate wafer-scale, high performance (high mobility, and high on/off ratio) thin film transistors for printed electronic applications. The parameters affecting device performance were studied in detail to establish a roadmap for the future of purified nanotube ink printed thin film transistors. The trade of between mobility and on/off ratio of such devices was studied and the effect of nanotube network density was explained in detail.

On the other hand, graphene transfer technology was explored here as well. Annealing techniques were utilized to deposit clean graphene on arbitrary substrates. Raman spectroscopy and Raman data analysis was used to confirm the clean process. Furthermore, suspended graphene membrane was fabricated using single and multi-layer graphene films. This can make a major impact on graphene based transistors and bio-nano sensors technology.

CHAPTER ONE

INTRODUCTION

1.1. MATERIAL STRUCTURE

It was in 1991 that Iijima found a new allotrope of carbon in shape of a cylindrical hollow tube [1]. Since then, carbon nanotube (CNT) has been a leading potential candidate for several science and technology applications.

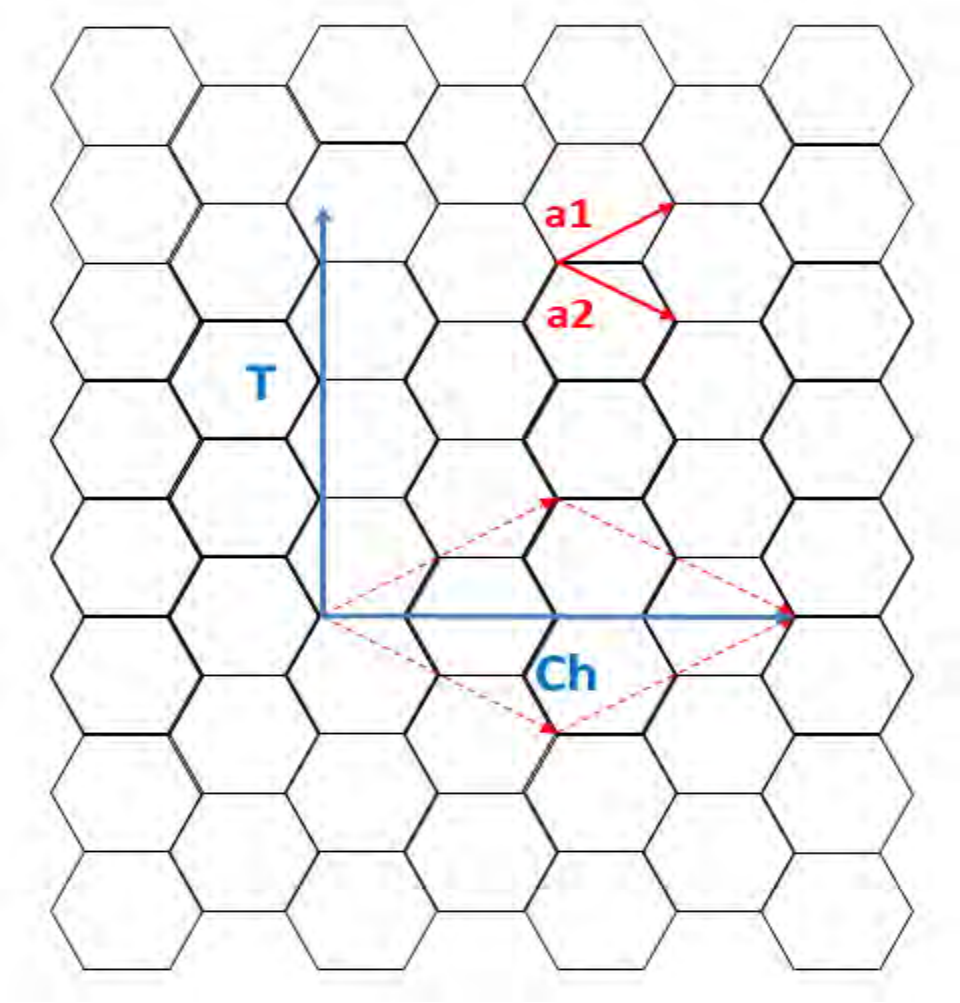

Figure 1.1. Graphene sheet to form SWNT

Single walled carbon nanotube (SWNT) is composed of a sheet of 1-atom-thick carbon, also known as graphene (sp^2 carbon honeycomb lattice), rolled into a seamless cylindrical shape [2].

Based on the cut and degree of twist of the graphene sheet (the *chirality*, specified by two indices (n,m)), SWNTs exhibit either metallic or semiconducting behavior. As shown in Figure 1.1 “Ch” is the chiral vector which demonstrates the circumference of the nanotube while “T” (translational vector) represents the direction of CNT.

$$Ch = n..\vec{a}1 + m.\vec{a}2 \quad (1)$$

where **a1** and **a2** are the unit vectors of the graphene sheet. On the other hand, the number of graphene sheets defines the number of tubes therefore there is also multi-walled carbon nanotubes made of more than one sheet of graphene rolled into concentric tubes. Owing to their unique material properties related to the one dimensional nature of electron transport, carbon nanotubes have been proposed for different electronic, chemical and mechanical applications. CNTs can be obtained using several techniques including chemical vapor deposition (CVD), laser ablation, and arc discharge. However, the precise control over the chirality of nanotubes during growth process is not yet observed.

Recently, graphene demonstrates great application potentials as a 2-dimentional material to be also used in electronic and sensor applications as well as mechanical and bio-membranes. Graphene has been discovered in 2004 through a very simple method of mechanical exfoliation [3]. Basically stacks of graphene sheets were peeled off of the graphite sample and then deposited randomly on the target substrate. To date, graphene films obtained using this technique are known as the best quality ones however, there is no control over the deposition location. To solve this problem several groups were able to grow graphene on Cu foil using CVD method [4] or on Ni film deposited on top of silicon wafer [5] and then transfer that to the preferred location

on arbitrary substrates. Nevertheless, the transfer process introduces contaminations and defects which in many ways affect the graphene film's quality and performance.

1.1.1. CNT: SCATTERING AND RESISTANCE

When a voltage applied across a carbon nanotube, there are several things involved in the resistance of the system. For a long nanotube (longer than the mean-free-path of electrons, l_{mfp}) the carrier flow falls into diffusive regime and resistance is expected to scale linearly with the length as in classical resistors [6]. However for nanotube length in the order of l_{mfp}, the ballistic transport occurs with the presence of an electric field.

For a 1d system in the ballistic limit, the resistance is greater than or equal to $h/e^2 = 25\ k\Omega$ (universal quantum resistance). For SWNT this number is divided by a factor of 4 (2 for electron spin options and 2 band structure degeneracy) therefore the contact resistance of SWNT is $R = h/4e^2$.

In general the DC resistance of a nanotube in diffusive regime is defined as

$$R_{total} = R_c + \frac{h}{4e^2} \cdot \frac{L_{CNT}}{l_{mfp}} \quad (2)$$

Where R_c is the contact resistance (to the outside electrode) and L_{cnt} is the nanotube length. Mean free path is however defined with the scattering rate in the nanotube. There are two sources of scattering in the nanotube: 1) *phonon scattering*, 2) *impurity scattering*.

Phonon scattering is the result of either the acoustic-phonon (for low bias voltages) or optical-phonon (high bias voltages) interaction which causes the electrons to scatter from their direction. Apparently this phenomenon highly depends on the temperature and deriving electric field, as the temperature increases the phonon scattering becomes more dominant. Besides, for high voltages the optical phonon scattering dominates resulting in current saturation in nanotubes. However, Impurity scattering comes from two sources of impurities, one is the impurities in the nanotube itself (including defect, doping, etc.) and the other one is the impurities in the substrate that can cause carrier scattering. Unlike phonon scattering, impurity scattering is not related to the temperature which makes it easier to observe phonon scattering effects by varying the temperature and voltage.

The total scattering is given by

$$\frac{1}{\tau_{total}} = \frac{1}{\tau_{ph}} + \frac{1}{\tau_{imp}} \quad (3)$$

here τ_{ph} and τ_{imp} are phonon and impurity scattering, respectively. Similarly, the mean free path relationship follows the same pattern with the phonon mean free path (l_{ph}) and impurity mean free path (l_{imp}). The impurity mean free path is in the range of 100 nm- 100 μm depending on the nanotube synthesize method and the substrate whereas phonon scattering is in the range of ~1 μm [6].

As a result, for nanotubes longer than the mean free path the resistance is approximately given by

$$R_{dc} \approx \frac{h}{4e^2}\frac{L_{CNT}}{l_{mfp}} \quad (4)$$

With the assumption of mean free path in range of 1 μm, the resistance of long nanotubes can be estimated as 6.25 kΩ/μm. Figure 1.2 shows the length scaling of resistance approaching the ballistic limit (6.25 kΩ, blue line) for short nanotubes. The comparison between Copper and SWNT resistance in two different temperature represents the future potential for nanotube interconnects replacing Cu interconnects.

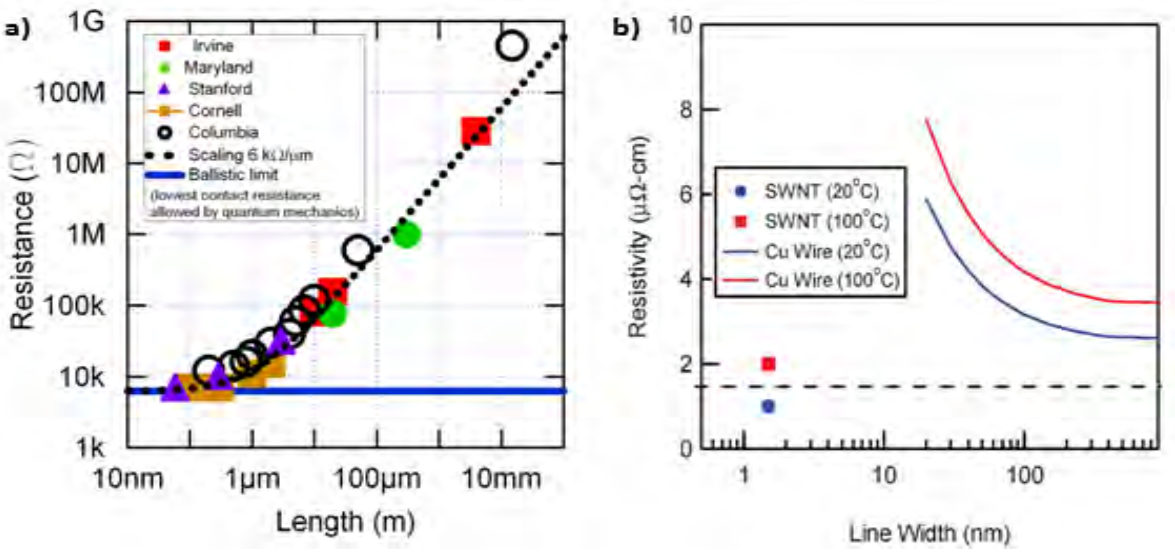

Figure 1.2. a) Resistance versus length for both diffusive and ballistic regimes. b) Comparison between SWNT and Cu resistivity in two different temperatures [6].

1.1.2. MOBILITY

Mobility is a term to characterize the movement of charge carriers (electron or hole) in any material when an electric field is applied. Mobility is based on the scattering properties of the

material which itself depends on the physical and molecular arrangement of that medium as discussed comprehensively in the previous section.

1-D structure of nanotubes results in near-ballistic transport of carriers in the tubes, so that mobility of individual nanotube is known to be around 10000 cm/V-s while for the random network of nanotube film this drops drastically below 100 cm/V-s [7, 8]. The principle question here is: What sets the mobility of a random network of semiconducting nanotubes with regard to individual nanotubes? Can "mobility" be increased by increasing the density? How does this affect the on/off ratio and what are the physical processes that set limits on this scaling?

To answer that, one should first review the theoretical fundamentals of mobility and the approaches used to calculate it. In practice, researchers mostly use the equation below to calculate the mobility which is obtained for small source-drain voltages (linear region),

$$\mu = \frac{\partial I_{DS}}{\partial V_{GS}} \frac{1}{V_{DS}} \frac{1}{C_{ox}} \frac{L_{SD}}{W} \quad (5)$$

However, it should be noted that commonly the devices are used in the saturation region. To make this feasible, one can use curve fitting to the device characteristic in the saturation region,

$$I_{DS} = \mu_0 W C_{ox} \frac{1}{L_{SD}} \left(V_{gs} - V_{th}\right)^2 \quad (6)$$

Another complication is the behavior of nanotubes in the network where there is a mixture of semiconducting and metallic nanotubes. So far, there is no practical method to have 100%

purified semiconducting nanotube network, thus the density of metallic tubes versus the overall density of network will add more obstacle in defining the mobility of such network. Additionally, the contact resistance, capacitance, and percolating effects should be taken into account which makes it difficult to quantitatively explore the mobility of non-purified or semi-purified nanotube network. As a result, a phenomenological experimental approach is required to progress in the investigation of mobility. In chapter 3, in depth discussion is presented on different theories to calculate the mobility and the fundamentals which set the mobility of a nanotube network.

Figure 1.3 shows a comparison between different state-of-the-art techniques used in device fabrication. As it can be seen here, individual SWNT can have high mobilities in the range of 10^4 cm^2/V-s while nanotube networks generally fall below 1000 cm^2/V-s. Although, a recent progress in dense, aligned synthesize of nanotubes on quartz substrate made it possible to push this limit beyond 10^3 cm^2/V-s [9, 10] but the on/off ratio is below 10 due to the presence of metallic tubes. In general, CVD-grown and solution deposited carbon nanotube network show 1-2 orders of magnitude lower mobility comparing to that of individual tubes. However, they still outperform a-Si and organic materials with a factor of 100x in mobility. Therefore, there is a great interest in investigating the performance of printed carbon nanotube devices. The remaining issue then would be the on/off ratio of nanotube networks made of mixture of semiconducting and metallic tubes. This in fact demonstrates the essential need in synthesize and purification techniques as will be discussed in chapter 3.

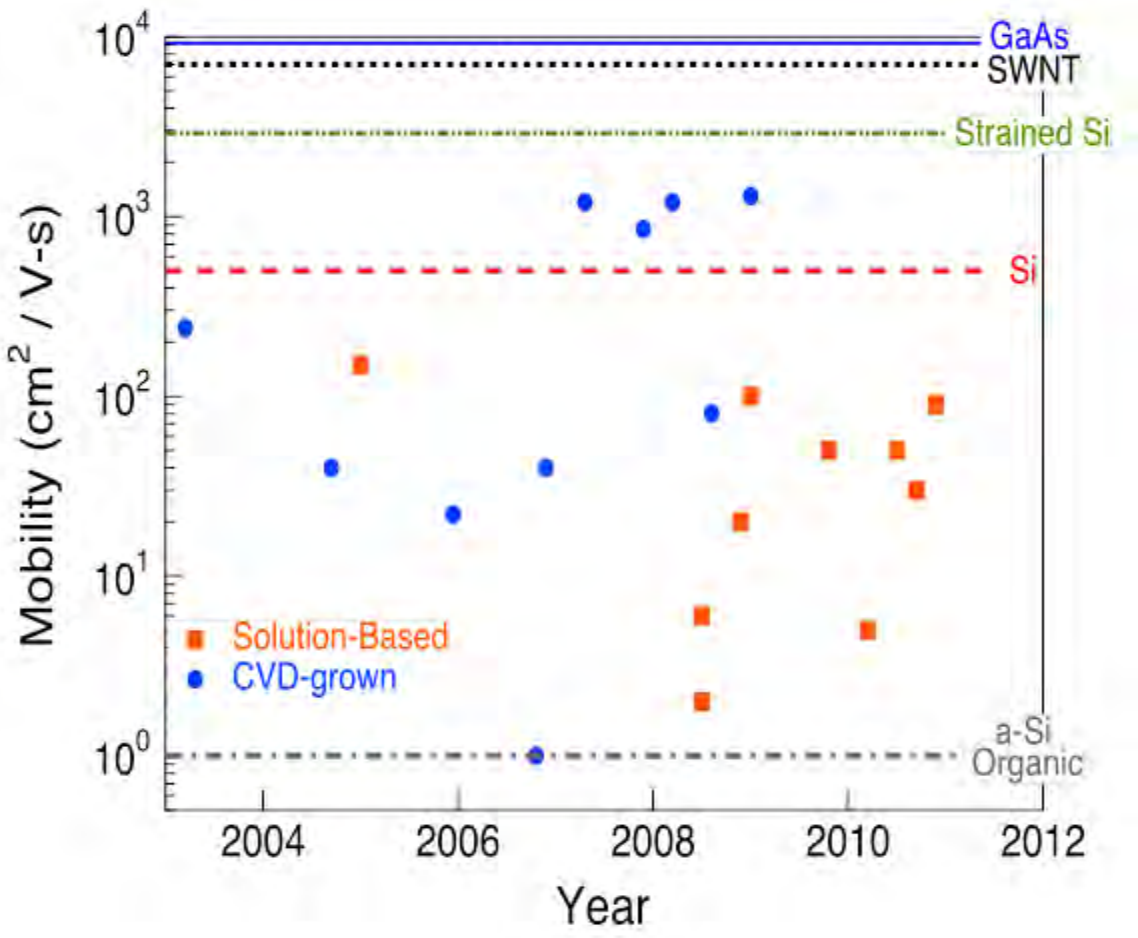

Figure 1.3. Mobility versus year for different state-of the art techniques

Graphene is also known to have high mobility in the range of 15000 cm^2/V-s [11] (with the intrinsic limit of ~200000 cm^2/V-s [12, 13]). However, the synthesize method is supposed to dramatically affect the mobility. According to experimental results, graphene sheets obtained from mechanical exfoliation demonstrate the best and highest mobilities. Another parameter affecting graphene's mobility is the substrate since it can introduce both phonon and impurity scattering which lowers the mobility. Therefore, suspended graphene is expected to have higher mobility than the same film laid on top of a substrate. Consequently, the study of suspended graphene membrane becomes a major point of interest in graphene based devices. Part of my

Ph.D. project was to establish a protocol to fabricate high yield suspended graphen membranes as will be discussed later. The preliminary electrical measurements demonstrate great potential for suspended membranes to be used in dual-electrolyte-gated transistors and biosensors for possible DNA sequencing techniques.

1.2. PROPERTIES AND APPLICATIONS

Carbon nanotubes have demonstrated outstanding potential for a wide range of applications, including field effect transistors and high-frequency electronics, chemical sensors, nanoelectromechanical systems (NEMS), thin film transistors and display electronics. Their small size, high mobility (near-ballistic electron transport), high intrinsic cut-off frequency, mechanical and thermal stability, high current carrying density and the capability of having both semiconducting and metallic tubes make carbon-based devices promising candidates to embed in (or replace in some cases in future) silicon-based devices in some applications [14].

One-dimension nanostructures, such as semiconducting nanowires and carbon nanotubes, have been heavily investigated as digital devices, but so far the study of such structures for RF applications is in its infancy. Although the field is still under development, we are beginning to understand some of the possible advantages of such systems over traditional, two-dimensional based technologies. Since 2003 it has been speculated that carbon nanotube devices have potentially terahertz cutoff frequencies [15, 16]. However, only recently have the device cutoff frequencies crossed into the gigahertz range, as reviewed in [14].

Field effect transistors based on dense, parallel arrays of nanotubes are currently being investigated in both academic and industrial laboratories [7-9, 14, 17-22]. To achieve the best possible performance, it is required that a uniform, aligned, and dense array of *all-semiconducting* nanotubes are on the substrate. Otherwise, the field-effect capacitance degrades the cut-off frequency and the mobility decreases from its intrinsic value [23]. Despite the fact that, so far, it is unlikely that perfectly dense and aligned arrays containing only semiconducting nanotubes needed for highest performance may be economically manufactured, it is critical to consider state-of-the-art results which have been used less-than-perfect nanotube networks. Despite being far from the theoretical limits of individual nanotubes, such results show attractive achievements and great improvements in device characteristics, as well as new horizons for applications in nanoelectronics, including large area printed electronics (that is, RFID tags) and flexible substrate systems.

Graphene on the other hand, due to its atomic structure (one-atom-thick layer), is known as the thinnest while most stable membrane available. The fascinating fact about graphene is that not only it can replicate the biological membranes due to its size, but also its mechanical stability and electrical conductivity makes it possible to extract data from the environment. Therefor it is among the best materials to be considered for biological, mechanical and chemical sensors. In addition to that, graphene offers new perspectives in THz electronics. So far, THz technologies were based on devices that operate in cryogenic environment, whereas graphene is expected to modulate a terahertz signal at room temperature. Graphene transistors recently show around 0.3 THz performance, which is outstanding among nano-transistors.

1.3. CHALLENGES AND METHODS

Carbon nanotubes using as-grown CNTs suffer from low on/off ratio as the device can hardly enter the off-state. The presence of metallic nanotubes in the channel will affect the performance of the transistor and present a short circuit path from source to drain electrode and, as a result, increases the off current and power consumption. Therefore, finding a technique that leads to the mass manufacturability of dense, aligned and *purified* semiconducting nanotube networks appears to be an essential step towards nanoelectronic devices. So far, purified solutions of carbon nanotube of more than 90% semiconducting (measured by spectroscopy techniques only) has been provided (Figure 1.4) using density gradient ultracentrifugation (DGU). However, the deposition technique and control over the performance of device fabricated using these nanotube inks are not yet clear. Carbon nanotube synthesize and purification techniques are also discussed more in detail in chapter 3.

One of the main remaining challenges is also to optimize the mobility and on/off ratio within an acceptable range suitable for both the high frequency and low power design. In this study I will present the methods used to tackle these issues. Generally, by controlling the density of nanotubes and the geometry of the devices one can alter the output of thin film transistors (TFTs). This will be discussed more in detail in the next two chapters.

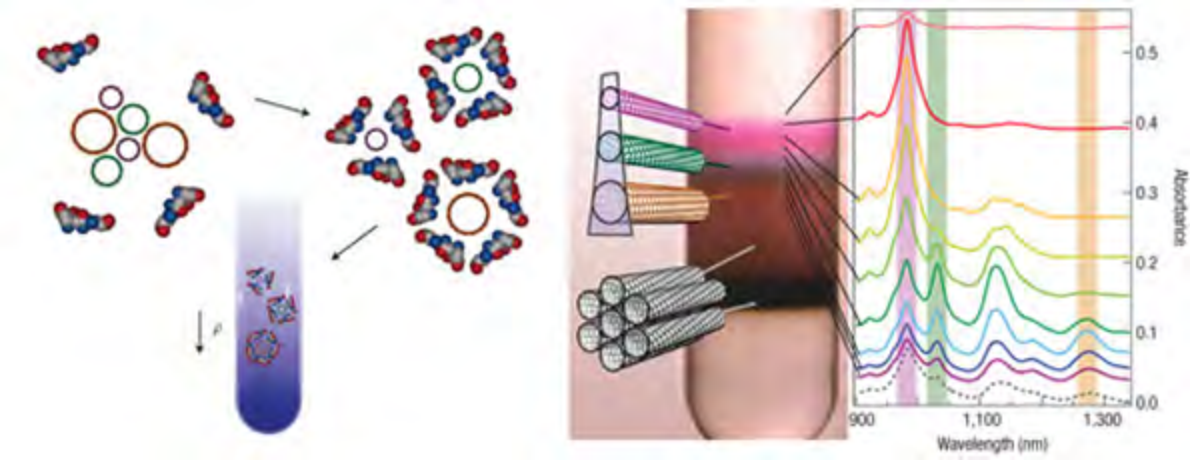

Figure 1.4. Carbon nanotube purification technique [24].

Apart from nanotube based transistors, graphene has also been studied here for potential electronic applications. One of the main challenges in graphene devices is to make a suspended graphene with no cracks and defects. So far according to the harsh environment in the fabrication procedure such as wet etching, suspended graphene films are having defects after transfer especially the ones with the bigger membrane size. We were able to establish annealing method to remove residues from the transfer process of graphene which was previously removed using wet process. Although graphene annealing was known, the impact of it on the Raman characteristic of the film has been investigated here. In addition, for the top liquid-gated graphene the main challenge is designing the microfluidic channel which imposes less stress on the membrane while offers the easy cleaning of the channel after each measurement. Same process was examined on to transverse microchannles with graphene membrane in between that seems to be a long-term goal and requires more considerations.

1.4. THESIS OVERVIEW

In this thesis I will present my research work in fabrication process and device analysis for carbon based (carbon nanotube and graphene) devices. My research work here is divided into two major parts, one is the carbon nanotube based devices and the second is graphene material used for membrane fabrication.

For the carbon nanotube based electronics I discuss the potential application of carbon nanotube for field effect and thin film transistors. The objective of this study is to explore the application of these devices in printed electronics and high frequency circuits as well as sensors. My main goal was pushing the limits for the performance of carbon nanotube based devices as well as presenting new applications. Meanwhile, I was able to demonstrate novel approaches to control the output characteristics of such devices with more understanding of their background operation. On the other hand, graphene has also been explored as a potential candidate to be used as thin membrane in electronic devices. Graphene's electronic properties together with its thickness and 2-dimentional structure make it a promising material for chemical and bio-nano sensors as well as liquid-gated transistors.

The first chapter covers the basic background of carbon nanotube and graphene material, properties, challenges, and applications.

In second chapter I will present the data obtained using Dielectrophoresis (DEP) method to deposit as grown pristine carbon nanotubes in the preferred location. The advantage of DEP is nanotube alignment based on the voltage and frequency applied to the carbon nanotube solution.

However, mainly DEP results in deposition of metallic tubes rather than semiconducting ones which will affect the performance of our devices as discussed later.

Chapter 3 discusses the main part of my project which involves, design, fabrication, characterization, and analysis of semiconducting carbon nanotube ink-based thin film transistors to be used mainly in printed electronic technology. In this work I used purified carbon nanotube ink with purity of more than 90% semiconducting tubes. The core achievement of this study was pushing the limits of device performance with regards to mobility and on/off ratio while introducing new techniques of controlling the output characteristics of such devices to be used in broad range of electronic applications. This investigation, for the first time, established the fundamental limits and studied key parameters that control the device outcome.

Chapter 4 focuses on graphene based devices starting with the development of graphene in our lab. The principles of graphene transfer techniques will be studied in this chapter. The primary objective of this chapter is to discuss the fabrication of suspended graphene to be used in future graphene membrane based sensors and field effect transistors.

Finally, in chapter 5 I will summarize my work with a discussion about the future perspectives.

1.5. REFERENCES

[1] S. Iijima, "Helical Microtubules of Graphitic Carbon," *Nature,* vol. 354, pp. 56-58, Nov 7 1991.

[2] J. W. G. Wildoer, L. C. Venema, A. G. Rinzler, R. E. Smalley, and C. Dekker, "Electronic structure of atomically resolved carbon nanotubes," *Nature,* vol. 391, pp. 59-62, 1998.

[3] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science,* vol. 306, pp. 666-669, Oct 22 2004.

[4] X. S. Li, W. W. Cai, J. H. An, S. Kim, J. Nah, D. X. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," *Science,* vol. 324, pp. 1312-1314, Jun 5 2009.

[5] A. Reina, X. T. Jia, J. Ho, D. Nezich, H. B. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, "Layer Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition," *Nano Letters,* vol. 9, pp. 3087-3087, Aug 2009.

[6] C. Rutherglen and P. Burke, "Nanoelectromagnetics: Circuit and Electromagnetic Properties of Carbon Nanotubes," *Small,* vol. 5, pp. 884-906, Apr 20 2009.

[7] N. Rouhi, D. Jain, K. Zand, and P. J. Burke, "Fundamental Limits on the Mobility of Nanotube-Based Semiconducting," *Advanced Materials,* vol. 23, pp. 94-99, Jan 4 2011.

[8] D. Jain, N. Rouhi, C. Rutherglen, C. G. Densmore, S. K. Doorn, and P. J. Burke, "Effect of Source, Surfactant, and Deposition Process on Electronic Properties of Nanotube Arrays," *Journal of Nanomaterials,* 2011.

[9] W. W. Zhou, C. Rutherglen, and P. J. Burke, "Wafer Scale Synthesis of Dense Aligned Arrays of Single-Walled Carbon Nanotubes," *Nano Research,* vol. 1, pp. 158-165, Aug 2008.

[10] J. L. Xiao, S. Dunham, P. Liu, Y. W. Zhang, C. Kocabas, L. Moh, Y. G. Huang, K. C. Hwang, C. Lu, W. Huang, and J. A. Rogers, "Alignment Controlled Growth of Single-Walled Carbon Nanotubes on Quartz Substrates," *Nano Letters,* vol. 9, pp. 4311-4319, Dec 2009.

[11] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature Materials,* vol. 6, pp. 183-191, Mar 2007.

[12] A. Akturk and N. Goldsman, "Electron transport and full-band electron-phonon interactions in graphene," *Journal of Applied Physics,* vol. 103, Mar 1 2008.

[13] S. V. Morozov, K. S. Novoselov, M. I. Katsnelson, F. Schedin, D. C. Elias, J. A. Jaszczak, and A. K. Geim, "Giant intrinsic carrier mobilities in graphene and its bilayer," *Physical Review Letters,* vol. 100, Jan 11 2008.

[14] C. Rutherglen, D. Jain, and P. Burke, "Nanotube electronics for radiofrequency applications," *Nature Nanotechnology,* vol. 4, pp. 811-819, Dec 2009.

[15] P. J. Burke, "An RF circuit model for carbon nanotubes," *IEEE Transactions on Nanotechnology,* vol. 2, pp. 55-58, Mar 2003.

[16] P. J. Burke, "AC performance of nanoelectronics: towards a ballistic THz nanotube transistor," *Solid-State Electronics,* vol. 48, pp. 1981-1986, Oct-Nov 2004.

[17] M. Steiner, M. Freitag, V. Perebeinos, A. Naumov, J. P. Small, A. A. Bol, and P. Avouris, "Gate-Variable Light Absorption and Emission in a Semiconducting Carbon Nanotube," *Nano Letters,* vol. 9, pp. 3477-3481, Oct 2009.

[18] P. Avouris, "Carbon nanotube electronics and photonics," *Physics Today,* vol. 62, pp. 34-40, Jan 2009.

[19] M. Engel, J. P. Small, M. Steiner, M. Freitag, A. A. Green, M. C. Hersam, and P. Avouris, "Thin Film Nanotube Transistors Based on Self-Assembled, Aligned, Semiconducting Carbon Nanotube Arrays," *Acs Nano,* vol. 2, pp. 2445-2452, Dec 2008.

[20] L. Nougaret, H. Happy, G. Dambrine, V. Derycke, J. P. Bourgoin, A. A. Green, and M. C. Hersam, "80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes," *Applied Physics Letters,* vol. 94, pp. -, Jun 15 2009.

[21] C. Rutherglen, D. Jain, and P. Burke, "rf resistance and inductance of massively parallel single walled carbon nanotubes: Direct, broadband measurements and near perfect 50 Omega impedance matching," *Applied Physics Letters,* vol. 93, pp. -, Aug 25 2008.

[22] C. Rutherglen and P. Burke, "Carbon nanotube radio," *Nano Letters,* vol. 7, pp. 3296-3299, Nov 2007.

[23] P. J. Burke, "Luttinger liquid theory as a model of the gigahertz electrical properties of carbon nanotubes (vol 1, pg 129, 2002)," *Ieee Transactions on Nanotechnology,* vol. 3, pp. 331-331, Jun 2004.

[24] M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, and M. C. Hersam, "Sorting carbon nanotubes by electronic structure using density differentiation," *Nature Nanotechnology,* vol. 1, pp. 60-65, Oct 2006.

CHAPTER TWO

NANOTUBE SOLUTION; SURFACTANT, AND DIELECTROPHORESIS DEPOSITION

2.1. INTRODUCTION

Carbon nanotubes can be used for both high performance electronics [1], printed electronics [2-4], and molecular sensors[5], as well as a host of other potentially exotic applications, such as nano-antennas [6, 7], molecular beacons [8], etc. However, a scalable manufacturing technology for nanotube devices with appropriate yield, reproducibility, and performance in various metrics (mobility, on/off ratio, cost, chemical sensitivity, sensor specificity, etc.) is currently lacking. This is, in part, due to the variety of synthesis and deposition techniques and challenges due to the inherent in nanotube physical properties.

Of these challenges, nanotube dispersion in solution followed by deposition into arrays or mats that preserves the intrinsic, high performance is the largest, unmet challenge. Thus, there is a great need for an integrated, comprehensive study of the effect of nanotubes synthesis procedures, dispersion procedures, and deposition processes on the electronic properties of nanotube arrays. Here we provide the first attempt at such a comprehensive study. While a complete understanding of the physical processes involved in these complex manufacturing steps is still lacking, our work provides the first, raw set of empirical guidelines to guide future technology development in this area.

2.1.1. DISPERSION

It is well known that synthesized carbon nanotubes (especially single walled carbon nanotubes, SWNTs) exist in the form of bundles, and that to exploit their electronic properties to the fullest a post processing technology is required to separate them into individual nanotubes. A common approach to achieve this is by stabilizing the hydrophobic nature of nanotube surface

with the use of a surfactant that overcomes the van der Waals forces among the nanotubes and results in suspensions of individual SWNTs.

It is also well known that all synthesis methods for single walled carbon nanotubes result in a mixture of chiralities and diameters, resulting in heterogeneous electrical properties, particularly a mixture of semiconducting and metallic nanotubes. In general it is assumed to be an even distribution of folding chiralities, 1/3 of all SWNTs in a sample being metallic with the remaining 2/3 exhibiting semiconducting behavior. The chemistry community has led a successful effort aimed at sorting and purifying nanotubes in solution post-synthesis [9].

To date, a wide variety of surfactants have been reported to be able to disperse the nanotube in bundles into their individual form in an aqueous media successfully [9, 10]. Several commercial surfactants, such as sodium dodecyl sulfate (SDS), sodium cholate (SC) and sodium dodecylbenzenesulfonate (SDBS) are among the most reported for an efficient dispersion. Most dispersion studies have been directed toward chemical modification of the nanotube surface. Although many researchers have tried to solubilize nanotube ends and exterior walls through various functionalization routes[11], dispersion via functionalization has found limited success. Furthermore, covalent functionalization disturbs the extended π-electron systems (sp^2 orbitals) of the nanotube surface, responsible for many attractive attributes of SWNTs. Therefore, non-covalent surfactants are desired.

At present, it is not known how these surfactants used for both the dispersion and metallic/semiconducting nanotube separation affect the electronic properties of nanotube arrays and films made from depositing nanotubes using various techniques. Adsorption of ionic surfactants on the surface could significantly modulate the device characteristics and affect the

conductance of the devices. It is critical to compare the electronic nature of the nanotube-surfactant conjugates versus intact nanotubes, since these reagents are increasingly being used in industry and laboratories. The objective in this research work was to investigate the effect of various surfactant and deposition techniques on nanotube electronic properties using carbon nanotubes synthesized and purified using a variety of methods from a variety of academic and industrial institutions.

2.2. DIELECTROPHORESIS THEORY

Several post synthesis processes involve solution based processing of nanotubes such as spin coating [12] or dielectrophoresis (DEP) deposition [13-15]. Spin-coating is considered as one of the best long-term approaches, but is not yet mature enough for ultra-dense arrays. Dielectrophoresis allows selective alignment of nanotubes into controlled locations, and so is used in this work as a test-bed for systematic studies of the effect of alignment, source, and surfactants on electronic properties of nanotube arrays.

In DEP deposition steps, the presence of both metallic and semiconducting carbon nanotubes in solution is the main hurdle to form single nanotube conductance channels. When an AC field is applied to the electrodes with nanotubes between the gap, the induced dipole moment of SWNTs interacts with non-uniform field resulting in a dielectrophoretic force which is influenced by the electronic properties of the SWNTs and in turn causes a separation of metallic and semiconducting nanotubes [16]. Assuming carbon nanotubes to be spherical particles for simplifying the equations, the dielectrophoretic force can be expressed as

$$\vec{F}_{DEP} \propto \varepsilon_m \frac{\varepsilon_p - \varepsilon_m}{\varepsilon_p + 2\varepsilon_m} \nabla E_{rms}^2 \quad (1)$$

where ε_p is the dielectric constant of the carbon nanotubes and ε_m is the dielectric constant of the solvent. At higher frequencies this force is basically proportional to the difference between dielectric constant of the carbon nanotubes and dielectric constant of the solvent. The force observed by metallic nanotubes is significantly larger than that on semiconducting nanotubes because of the high dielectric constant of metallic SWNTs and the low dielectric constant of semiconducting SWNTs. When a solvent with a dielectric constant between those values is used, separation of SWNTs will occur with metallic SWNTs attracted towards the field source (positive DEP) and semiconducting SWNTs repelled from the source (negative DEP). This physical effect results in separation of nanotubes due to metallic nanotubes being attracted towards field source electrodes while leaving behind semiconducting nanotubes in solution.

In this work, we use DEP for the deposition process. Therefore, our studies tend to elucidate primarily arrays of metallic SWNTs. However, these initial pioneering studies are meant to provide qualitative guidelines for the effects of surfactants & synthesis recipes on all types of SWNT arrays, including random and aligned arrays of all-semi, all-metal, or mixed species of SWNTs. Such studies are urgently needed if nanotube electronics is to progress from science to technology.

2.3. DEVICE FABRICATION

2.3.1. NANOTUBE PREPARATION

Single walled carbon nanotubes were obtained from several different sources. Nanotubes obtained differ in terms of synthetic procedure used for their fabrication. Table 1 contains a list of nanotubes sources we used with some details of their basic properties.

Table 2.1. Nanotube sources and their properties

Company	Synthetic Process used	Average Diameter (reported by provider)
CNI/Unidym	HiPCO	0.81-0.85 nm
SouthWest Nanotechnologies	CoMoCAT	0.8-1 nm
Carbon Solutions	Arc discharge	1-1.4 nm
Las Alamos (semi-enriched)	HiPCO	0.81-0.85 nm
Cheap Tubes	CVD	1-2 nm
Nanointegris (semi-enriched, 90%)	Arc discharge	1.2 -1.6 nm

Nanotube diameters as mentioned in this table are obtained from the datasheets provided by their supplier and are also listed on their websites. Each of these nanotubes (except semi-enriched samples from Los Alamos[17]) and semi-enriched (90% semi-conducting) solution obtained from Nanointegris, were first dispersed in surfactant solutions. Surfactants used for the

comparison in our experiments were SDS, SC and SDBS. The protocol used for the dispersion of each sample is as follows:

1. 5% w/v (weight/volume) solutions of surfactants were prepared in DI water.
2. 5 mg of nanotube sample was dispersed in 10 mL of surfactant solution.
3. Suspensions formed after addition of nanotubes were then sonicated for 3 hours.
4. Mixtures were then centrifuged at 16,400 rpm (@ 30 °C) for 1 hour, 6 times repeatedly.

Dispersions obtained after 6 times centrifugation were then used for the deposition. Purified nanotubes obtained from Las Alamos were first dialyzed with 1% SDS solution in deionized water prior to their use. Nanointegris nanotube solution was used as received.

2.3.2. FABRICATION METHODS

High resistivity silicon wafer (8000 Ω-cm) with a 500 nm thermal oxide layer was used as the substrate. Since the next steps in the procedure involve high frequency input signals, high resistivity wafer reduces the loss in the substrate. Subsequently, using photolithography, electrodes were patterned in a coplanar waveguide (CPW) configuration. Shipley 1827 photoresist were spun on the substrate with 3500 rpm, this creates a photoresist film with a thickness of around 2.5 μm. Photoresist was then pre-baked in the 90 ^{o}C oven for about 25 minutes to get rid of solvents in the photoresist. The samples were patterned using MA-6 mask aligner with 10 mW for about 12-15 sec (~140 Jouls). Following that, samples were put in MF-319 for ~40 sec (or until visually confirmed) to develop the photoresist. Now the sample is ready for electrode deposition. E-beam evaporation was used to deposit Ti/Au (5/50 nm) electrodes (at a very slow rate of 0.1-1 A^{o}/sec; lower rates at the beginning of deposition and higher rates

towards the end. Devices were then dipped into fresh Acetone for lift-off until the unwanted metal peel off leaving the patterned electrodes behind.

2.3.3. DIELECTROPHORESIS

Using a glass micropipette with a tip diameter of ~20 µm, the nanotube solution drop was placed on the electrodes and DEP was used to accumulate the solubilized SWNTs within the electrode gap. This was accomplished using a 1 – 5 V_{pp}, 300 KHz – 25 MHz sine wave voltage signal applied to the electrodes. The drop was then air dried and the residue from the solution left after evaporation was gently washed away with deionized water. Figure 2.1 shows the layout for our measurements.

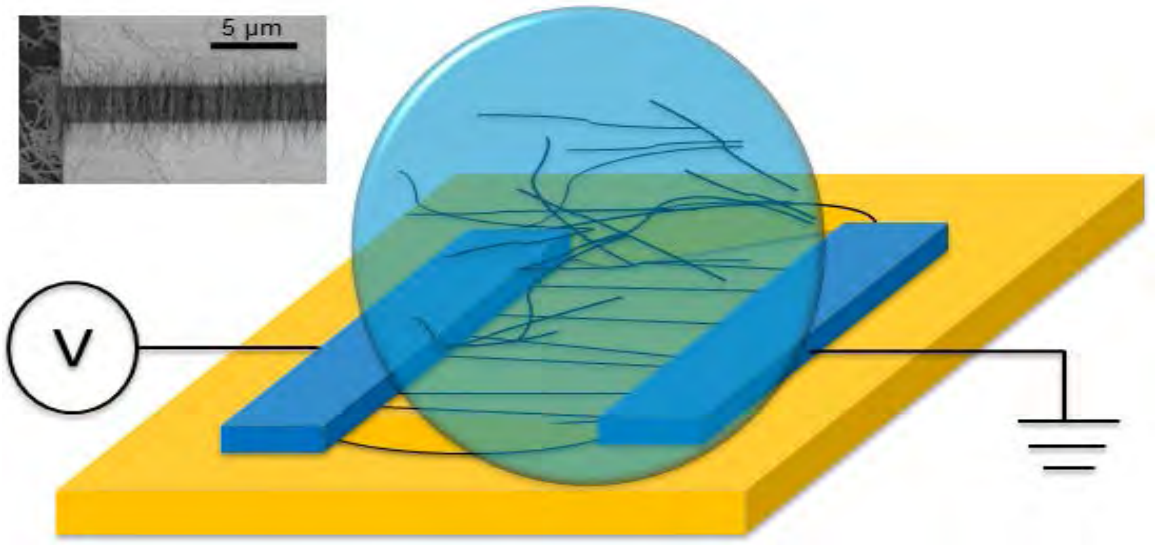

Figure 2.1. RF probing of dual CPW (co-planar waveguide)/electrode structure.

After accumulation of aligned SWNTs within the gap by DEP, contact electrodes were patterned on top of the nanotube film, connecting them to the bigger finger electrodes, using e-beam lithography and evaporated with 70 nm of Palladium (Pd) producing a final electrode gap

of 1 μm. Palladium has work function (~5.1 eV) higher than the SWNT (~4.9 eV) therefore is known to make an ohmic contact rather than schottky. The devices were rf-electrically contacted using a commercially available probe. Figure 2.2 shows a schematic diagram of several steps involved in the process of making a device with nanotubes deposited in the gaps.

Rather than characterizing each device in full detail, we opted for a simplified, higher throughput measurement procedure in order to maximize the number of deposition conditions we could perform. For all the dc resistance measurements, a low source-drain bias voltage (+1 V to -1 V) was used. Gate voltages of -9, 0 and +9 V were applied to the oxide layer (bottom gate, 500 nm) to modulate the conductance and measure the on/off ratio for the nanotube devices. Because the full depletion curve was not measured, the on/off ratio is qualitative, not quantitative. (The devices may not have been completely “on” or “off” in our simplified measurement scheme.)

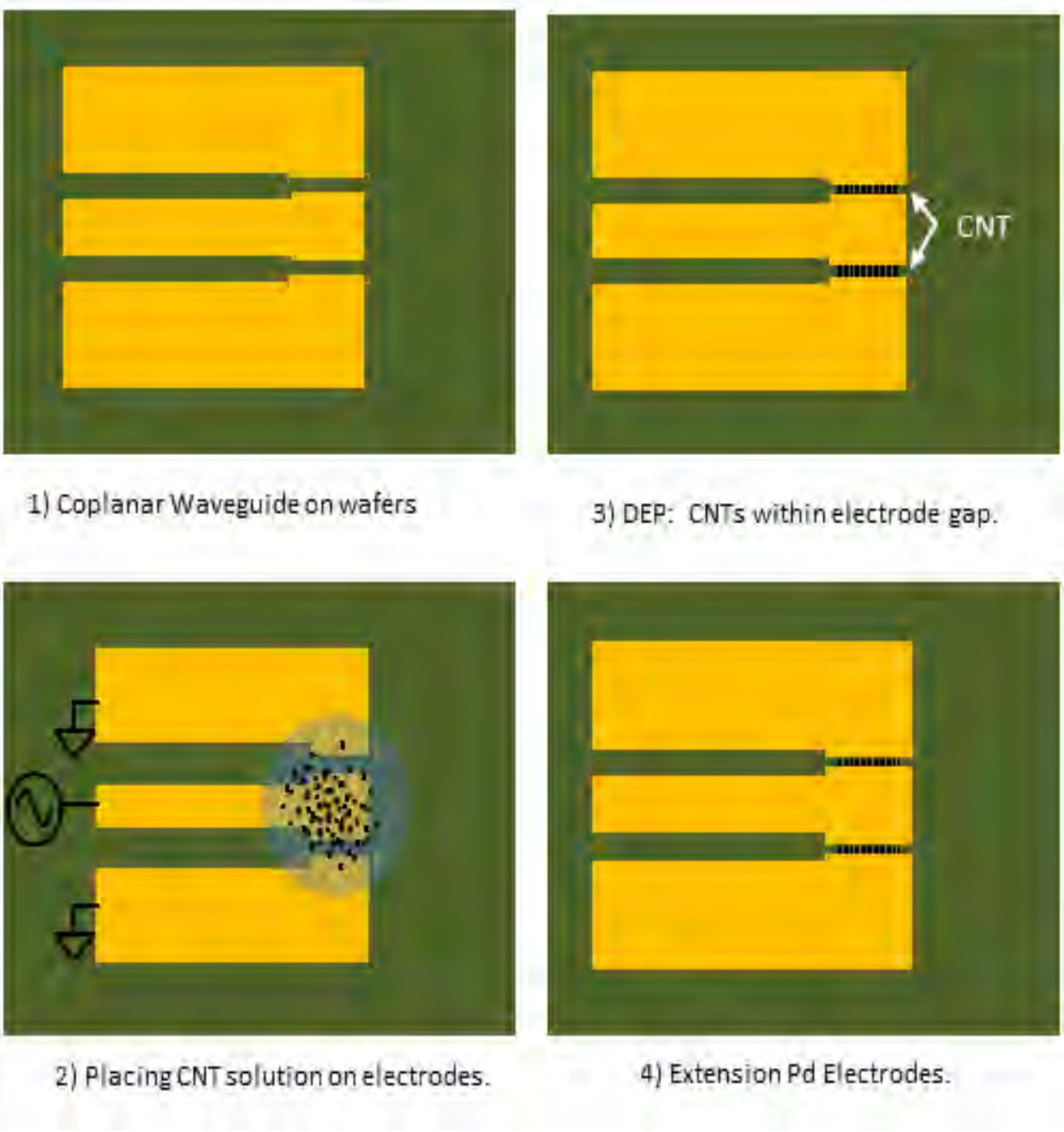

Figure 2.2. Fabrication steps used for DEP deposition of nanotubes

2.4. EXPERIMENTAL RESULTS

Electronic measurements were performed on several devices fabricated while keeping some factors common for comparison. Based on our experiments we have identified the role of frequency and amplitude used in DEP for the deposition of nanotubes. We were able to optimize these factors to make such device fabrication reproducible to a certain extent. These results help researchers to establish a similar protocol for optimized deposition when nanotubes are obtained from different sources.

The following comparison results are based on the data obtained by averaging results for several similarly formed devices. DC resistance values are normalized for a device with a width of 100 μm. The length of devices was kept in the range of the length of nanotubes from respective sources (Table 2).

2.4.1. COMPARISON ON NANOTUBE SOURCES

Nanotubes obtained from various sources were deposited on wafers and electronic measurements are summarized here. Nanotubes obtained from Unidyn (formerly Carbon Nanotechnologies Inc, HiPCO, 0.81 - 0.85 nm diameter, length <1 μm) were found to show greater resistance as compared to the lowest shown by nanotubes from Cheap Tubes Inc. (Arc discharge, 1 - 2 nm diameter, length >3 μm). Figure 2.3 shows a cumulative chart on dc resistance studies done on nanotubes that differ in their synthetic process. For our experiments, we obtained nanotubes from different sources to accommodate nanotubes produced by HiPCO, CoMoCAT, Arc and CVD methods. In these experiments, 4 V_{pp}, 25 MHz sine wave input voltage was applied for 3 minutes to the electrodes for the deposition of nanotubes.

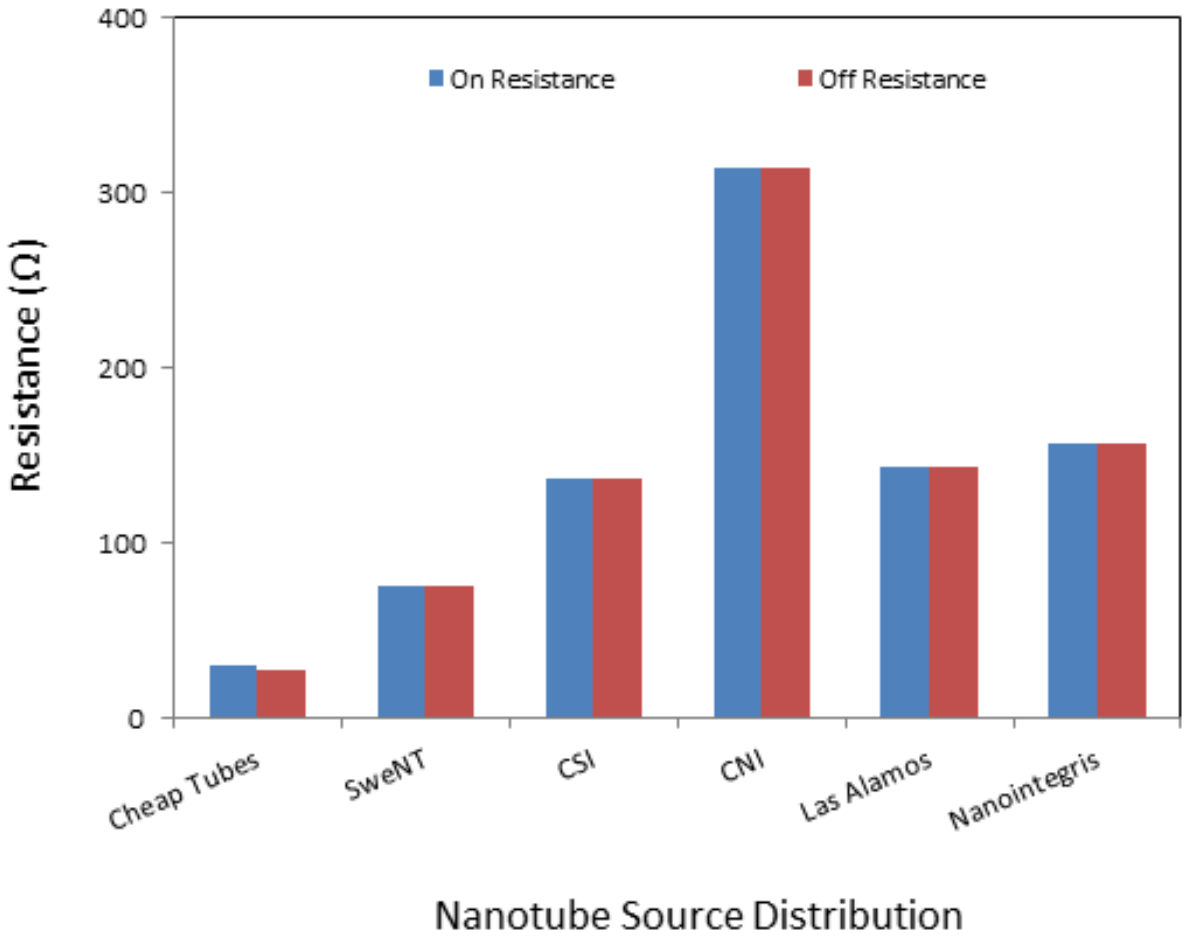

Figure 2.3. Results of dc resistance measurements done on nanotubes obtained from various sources that differ in synthetic process used (HiPCO/CoMoCat/Arc/CVD)

2.4.2. COMPARISON ON USING DIFFERENT SURFACTANTS

Three different surfactants – Sodium Cholate (SC), Sodium dodecyl Sulfate (SDS) and Sodium Dodecyl Benzene Sulfonate (SDBS) were used to solubilize nanotubes in aqueous solution. SC was found to be most effective surfactant for solubilizing most of the nanotubes. Figure 2.4 shows the on/off dc resistance of nanotube devices where nanotubes from several sources were dissolved using different surfactants and deposited on wafers using DEP. In all

experiments, 4 V_{pp}, 25 MHz sine wave voltage signal was applied for 3 minutes to the electrodes for the deposition of nanotubes.

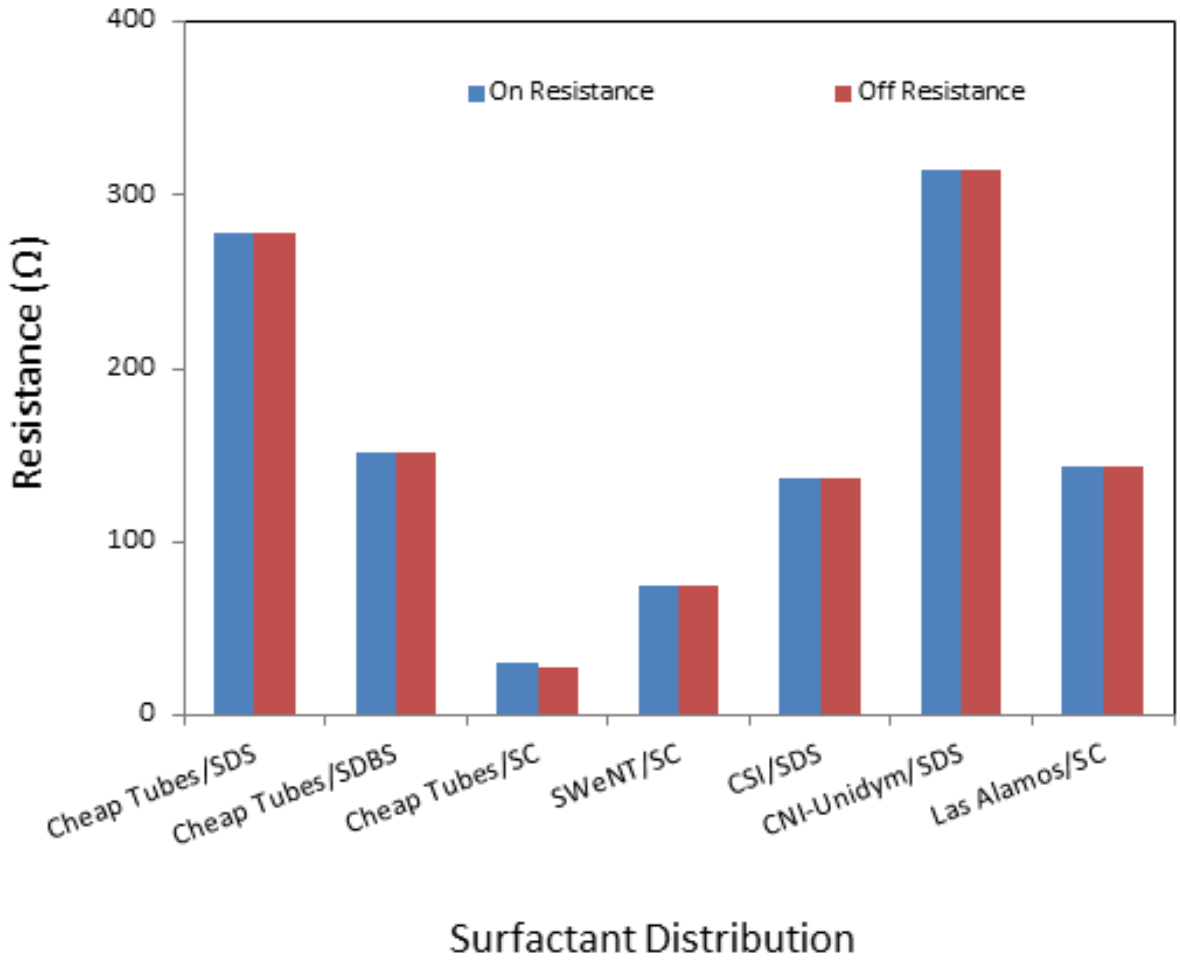

Figure 2.4. Results of dc resistance measurements done on nanotubes solubilized using variety of surfactants SDS, SC and SDBS

2.4.3. COMPARISON ON USING DIFFERENT FREQUENCIES

When different frequencies were used for the deposition, it was observed that nanotubes deposited using a frequency less than 15 MHz were not aligned, while when a frequency above 25 MHz was used, deposited nanotubes were found to be well aligned. Figure 2.5 shows some

representative images of nanotubes deposited under various different conditions. Several different patterns of alignments were observed owing to different DEP parameters. Figure 2.5a,b shows DEP deposition in 2 MHz frequency (no good alignment) versus Figure 2.5c,d with frequency of 25 MHz (high degree of aligment). In one case it was also observed that when a nanotube solution (nanotube dispersed in 1% w/v solution of SC) was left standing prior to its use for DEP deposition for several days, nanotubes formed bigger bundles, which were apparent in their SEM images (Figure 2.5 e,f).

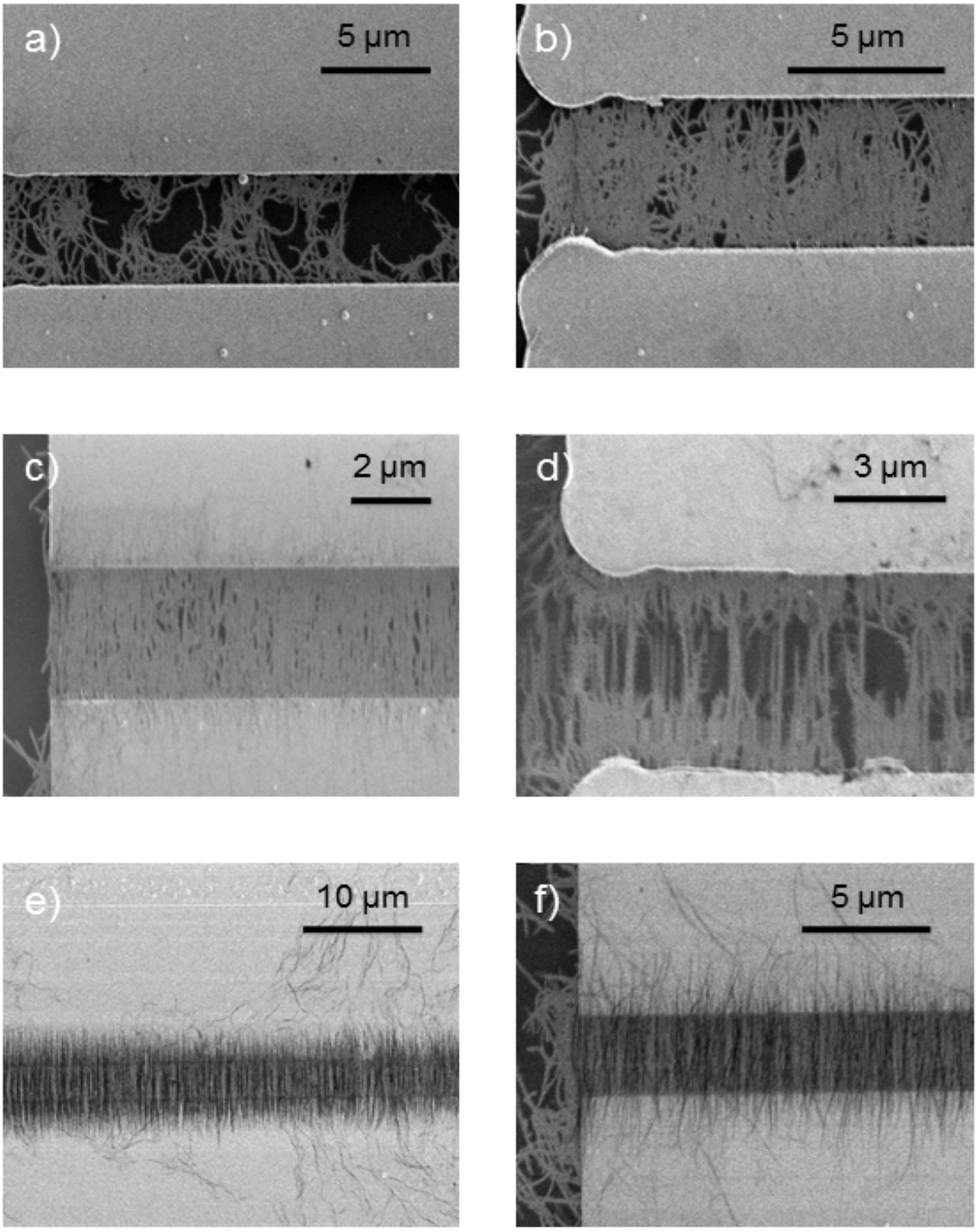

Figure 2.5. Nanotubes (Cheap Tubes) deposited on Si wafers at 2 MHz (a, b) and 25 MHz (c, d). The difference in their alignment is apparent. d) Deposited nanotubes (25 MHz) shorter in length (< 2 µm), it can be seen that even shorter nanotubes were amazingly aligned in the gap. e, f) nanotubes deposited from a solution that was sonicated for a short time (5 min) and then left standing for a few days prior to use, formation of bigger bundles of nanotubes are apparent in the images.

2.4.4. COMPARISON ON USING DIFFERENT AMPLITUDE

Nanotube samples (Cheap Tubes, dissolved using SC) were deposited by applying several different voltages for DEP at a constant frequency of 25 MHz. In general it was observed that when amplitude above 3 V was applied, 2 minutes or more was sufficient to fill the gap up to almost 100%. When a voltage less than 1 V was used, no nanotubes were apparently deposited. Using a dilute solution and giving more time for the deposition or using a comparatively concentrated solution with less time yielded the devices with similar properties. Also using any amplitude above 3 V did not make significant difference on device characteristics.

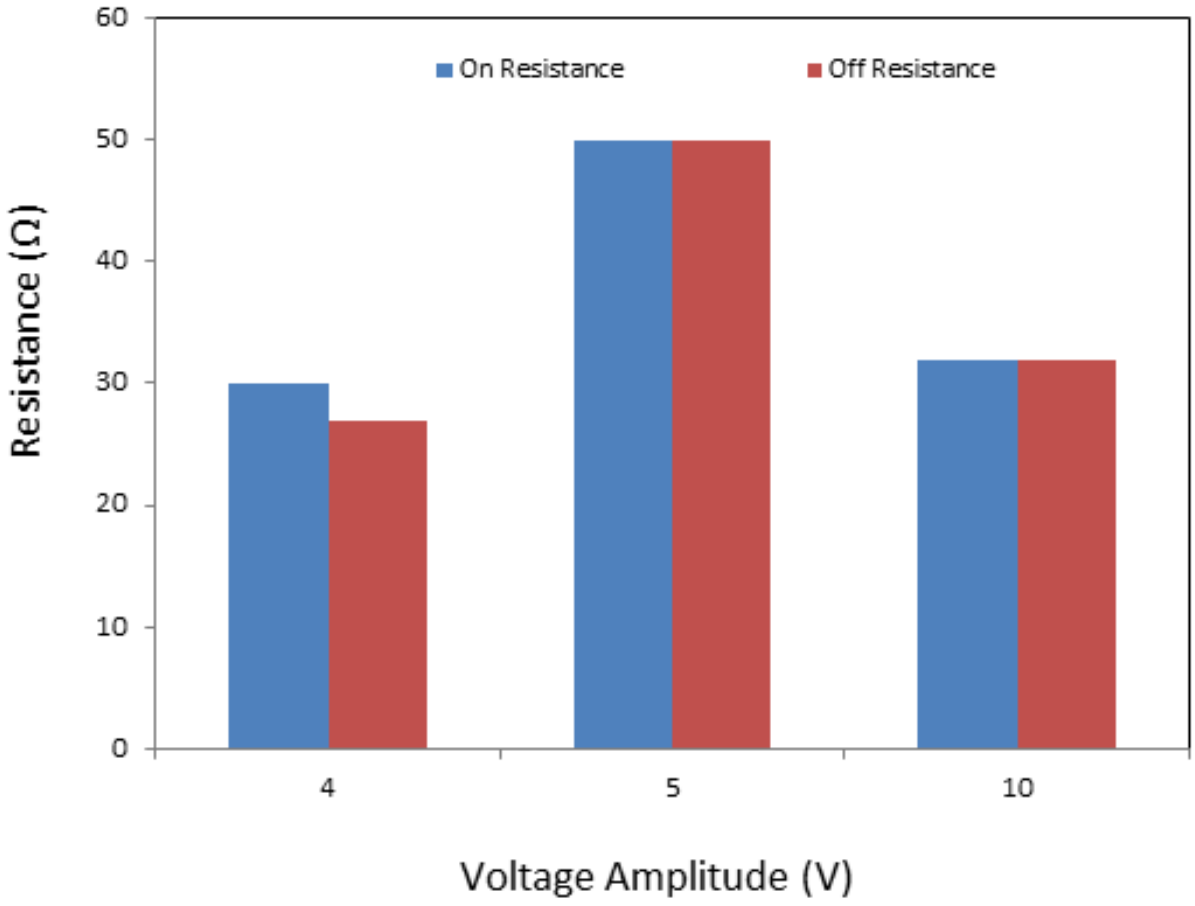

Figure 2.6. DEP depositing of nanotubes using different amplitudes

Figure 2.7 below shows a typical Raman spectrum from a device (with nanotubes from Cheap Tubes), indicating that indeed SWNTs are being deposited.

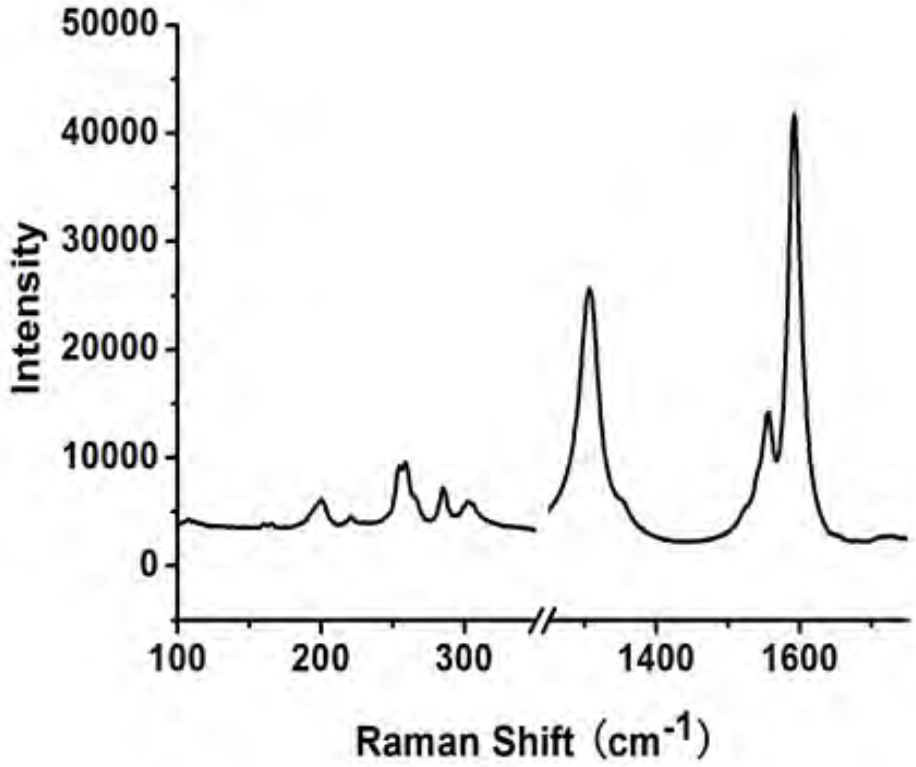

Figure 2.7. Raman spectra from a device representative shown in Figure 2.5, confirms the presence of nanotubes

2.4.5. REPRODUCIBILITY

Figure 2.8 presents a histogram plotted for dc resistance measurement done on several devices with different width. Most of the devices having the same width had shown dc resistance in similar range (Figure 2.8a), which shows the reproducibility of our experiments. Figure 2.8b plots averaged dc resistance as a function of devices' electrode width. Increasing the width 10 times in fact lowered the resistance with an order of 10, which shows the reliability of the process in terms of reproducing the results over the repeated experiments.

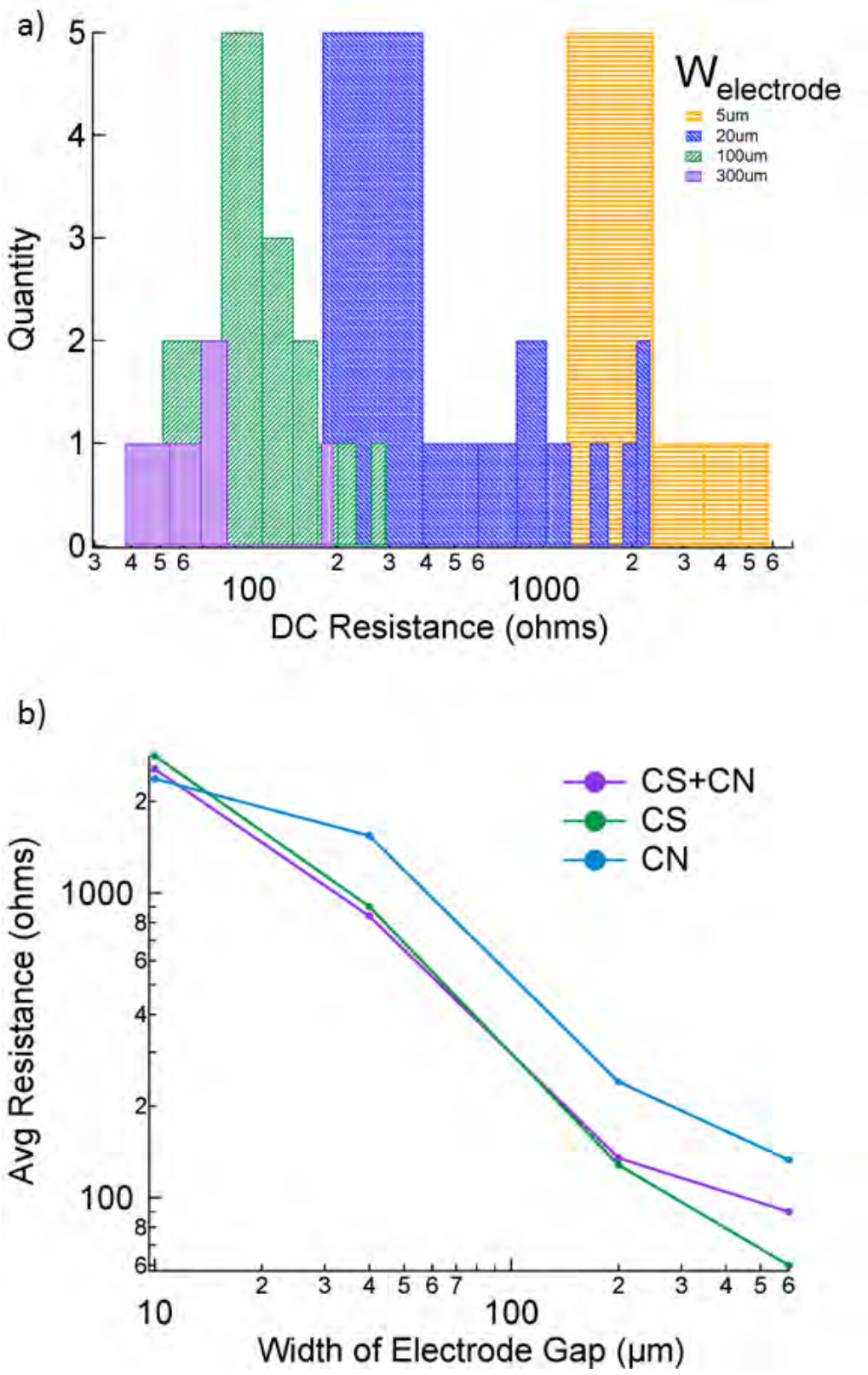

Figure 2.8. Averaged DC resistance measurement for devices with different electrode width

2.5. DISCUSSION

Use of ionic surfactant to solubilized nanotubes is known to modulate the surface conductance of nanotubes that will eventually affect the dielectrophoresis force applied for the deposition of nanotubes. Strano's group studied effects of surface conductivity of semiconducting SWNTs induced by ionic surfactants on the sign of dielectrophoretic force [18]. They were able to modulate the surface conductance by changing the ionic strength of medium. Also by neutralizing the surface charge using an equimolar mixture of anionic and cationic surfactant, they observed negative DEP of semiconducting species at 10 MHz. They suggested 10 MHz to be the crossover frequency for their semiconducting nanotube. From our experiments we found that in most of the cases when nanotubes were deposited at frequencies higher than 5 MHz, only metallic behavior of deposited nanotubes was observed in the electronic measurements. Even when the solution enriched in semiconducting nanotube was used, dielectrophoretic deposition at a frequency higher than 5 MHz resulted in devices with extremely low or no on/off ratio. We believe this is because even if above crossover frequencies semi-conducting nanotubes might have observed positive DEP.

The on/off ratios reported here are consistent with other works that found that when a conventional SWNT solution with ~ 2/3 of semiconducting nanotubes are deposited using DEP, major part of the dc current (90-95%) is produced by metallic nanotubes [19, 20]. They also found when 99% semi-enriched solution was used for deposition with DEP along with substrate's surface modification, the devices didn't go to complete off state, most likely because a small amount of metallic nanotubes were preferentially deposited by DEP [3, 20]. In another recent experiments [2, 3, 21], we used same semi-enriched solution (90%, Nanointegris),

deposited them without DEP by using only surface modification which resulted in devices with better mobility and also higher on/off ratios than the current DEP method. The on/off ratio of up to more than 100000 was achieved when nanotubes were deposited using only surface modification [2, 3].

Table 2.2. Summary of results

SWNT Sources	Electrode spacing	Avg. length after deposition (in SEM)	DC resistance (1000's of SWNTs in parallel)	On/off ratio
Cheap Tubes	3 µm	> 3 µm	< 50 (Ohms)	2-8%
SWeNT	1 µm	< 1 µm	50-100 (Ohms)	2-6%
CSI	1 µm	<1.5 µm	100-200 (Ohms)	<1%
CNI/Unidym	1 µm	<1 µm	100-500 (Ohms)	<1%
Las Alamos	1 µm	<1.5 µm	120-150 (Ohms)	<1%
Nanointegris (semi-enriched, 90%)	1 µm	<1.5 µm	150-180 (Ohms)	<1%

2.6. CONCLUSION

We have performed the first systematic study of the effects of surfactants, source, and DEP deposition procedure on nanotube electronic properties. In our experience, neither the surfactant used, nor the source, have a significant impact on the "on" resistance. The alignment is very

effected by the frequency of the ac voltage used to align the nanotubes. On the other hand, a consistent scaling of device resistance with width is observed for samples from different sources, indicating that the procedure can be empirically adjusted to give reasonably tight tolerances. Using this technique, the on/off ratio was never large, indicating that mostly metallic nanotubes were deposited in the DEP technique. Finally, we consistently (with almost perfect yield) were able to achieve devices with resistance of order 50 Ohms, regardless of nanotubes source or surfactant, which holds promise for future RF devices with nanotube arrays.

2.7. ACKNOWLEDGMENT

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2.8. REFERENCES

[1] C. Rutherglen, D. Jain, and P. Burke, "Nanotube Electronics for RF Applications," *Nature Nanotechnology*, 2009.

[2] N. Rouhi, D. Jain, K. Zand, and P. J. Burke, "Fundamental Limits on the Mobility of Nanotube-Based Semiconducting," *Advanced Materials*, vol. 23, pp. 94-99, Jan 4 2011.

[3] N. Rouhi, D. Jain, and P. Burke, "High-Performance Semiconducting Nanotube Inks: Progress and Prospects," *ACS Nano*, 2011.

[4] Q. Cao and J. Rogers, "Ultrathin Films of Single-Walled Carbon Nanotubes for Electronics and Sensors: A Review of Fundamental and Applied Aspects," *Advanced Materials*, vol. 21, pp. 29-53, 2009.

[5] P. G. Collins, K. Bradley, M. Ishigami, and A. Zettl, "Extreme oxygen sensitivity of electronic properties of carbon nanotubes," *Science*, vol. 287, pp. 1801-1804, MAR 10 2000.

[6] P. J. Burke, S. D. Li, and Z. Yu, "Quantitative theory of nanowire and nanotube antenna performance," *Ieee Transactions on Nanotechnology*, vol. 5, pp. 314-334, Jul 2006.

[7] P. J. Burke, C. Rutherglen, and Z. Yu, "Carbon Nanotube Antennas," *Proceedings of the 9th International Conference on Electromagnetics in Advanced Applications*, p. 937, 2005.

[8] H. Jin, D. Heller, and M. Strano, "Single-Particle Tracking of Endocytosis and Exocytosis of Single-Walled Carbon Nanotubes in NIH-3T3 Cells," *Nano Letters*, vol. 8, pp. 1577-1585, 2008.

[9] M. Hersam, "Progress towards monodisperse single-walled carbon nanotubes," *Nature Nanotechnology*, vol. 3, pp. 387-394, 2008.

[10] V. C. Moore, M. S. Strano, E. H. Haroz, R. H. Hauge, R. E. Smalley, J. Schmidt, and Y. Talmon, "Individually Suspended Single-Walled Carbon Nanotubes in Various Surfactants," *Nano Lett.*, vol. 3, pp. 1379-1382, 2003.

[11] C. A. Dyke and J. M. Tour, "Covalent functionalization of single-walled carbon nanotubes for materials applications," *Journal of Physical Chemistry A*, vol. 108, pp. 11151-11159, Dec 23 2004.

[12] M. C. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim, and Z. N. Bao, "Self-sorted, aligned nanotube networks for thin-film transistors," *Science*, vol. 321, pp. 101-104, Jul 4 2008.

[13] R. Krupke, F. Hennrich, H. B. Weber, M. M. Kappes, and H. von Lohneysen, "Simultaneous deposition of metallic bundles of single-walled carbon nanotubes using ac-dielectrophoresis," *Nano Letters*, vol. 3, pp. 1019-1023, AUG 2003.

[14] C. Rutherglen, D. Jain, and P. Burke, "RF resistance and inductance of massively parallel single walled carbon nanotubes: Direct, broadband measurements and near perfect 50 ohm impedance matching," *Applied Physics Letters*, vol. 93, p. 083119, 2008.

[15] D. Jain, N. Rouhi, C. Rutherglen, C. G. Densmore, S. K. Doorn, and P. J. Burke, "Effect of Source, Surfactant, and Deposition Process on Electronic Properties of Nanotube Arrays," *Journal of Nanomaterials*, 2011.

[16] R. Krupke, F. Hennrich, H. von Lohneysen, and M. M. Kappes, "Separation of metallic from semiconducting single-walled carbon nanotubes," *Science*, vol. 301, pp. 344-347, Jul 18 2003.

[17] S. Niyogi, C. G. Densmore, and S. K. Doom, "Electrolyte Tuning of Surfactant Interfacial Behavior for Enhanced Density-Based Separations of Single-Walled Carbon Nanotubes," *Journal of the American Chemical Society*, vol. 131, pp. 1144-1153, Jan 28 2009.

[18] Y. Kim, S. Hong, S. Jung, M. S. Strano, J. Choi, and S. Baik, "Dielectrophoresis of surface conductance modulated single-walled carbon nanotubes using catanionic surfactants," *Journal of Physical Chemistry B*, vol. 110, pp. 1541-1545, Feb 2 2006.

[19] A. Le Louarn, F. Kapche, J. M. Bethoux, H. Happy, G. Dambrine, V. Derycke, P. Chenevier, N. Izard, M. F. Goffman, J. P. Bourgoin, V. Derycke, P. Chenevier, N. Izard, M. F. Goffman, and J. P. Bourgoin, "Intrinsic current gain cutoff frequency of 30 GHz with carbon nanotube transistors," *Applied Physics Letters*, vol. 90, p. 233108, Jun 4 2007.

[20] L. Nougaret, H. Happy, G. Dambrine, V. Derycke, J. P. Bourgoin, A. A. Green, and M. C. Hersam, "80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes," *Applied Physics Letters*, vol. 94, p. 243505, Jun 15 2009.

[21] N. Rouhi, D. Jain, K. Zand, and P. J. Burke, "All-semiconducting nanotube devices for RF and microwave applications," *Proceedings of the IEEE MTT International Microwave Symposium*, May 2009.

CHAPTER THREE

SEMICONDUCTING NANOTUBE INK BASED THIN FILM TRANSISTORS

3.1. INTRODUCTION

In the previous chapter the work on DEP deposition of nanotube ink was presented. The ink consisted of mixture of metallic and semiconducting nanotubes, and because of the DEP deposition technique we used it has been observed that mainly the nanotubes in the channel (gap between electrodes) were metallic rather than semiconducting therefore the devices had on/off ratio of not more than 2,3 in almost all cases. However, to fabricate high mobility, high frequency, low power (low on/off ratio) transistors one need to lay down semiconducting film of CNTs. But first we need to obtain the base material which is the semiconducting nanotube film.

What are the milestones in obtaining semiconducting nanotube network? The answer to this question lies ultimately with the atomic structure of an individual single walled carbon nanotube (SWNT), composed of a sheet of graphene (sp^2 carbon honeycomb lattice) rolled into a seamless cylindrical shape [1]. As mentioned earlier, based on the cut and degree of twist of the graphene sheet (the *chirality*, specified by two indices (n,m)), SWNTs exhibit either metallic or semiconducting behavior. Owing to their unique materials properties related to the one dimensional nature of electron transport, carbon nanotubes have been proposed for different electronic applications including RF devices [2], digital logic circuits [3, 4], interconnects [5] and conductive sheets [6]. However, the key challenge which occurs over and over in all of carbon nanotube science and technology is the ability to economically control the position and composition of macroscopic numbers of nanotubes in a way which preserves the outstanding electrical properties of pristine, individual SWNTs.

Several approaches have been tried to demonstrate different fabrication techniques for depositing nanotubes at preferred locations on substrates in order to obtain high performance

nanotube-based circuits and devices. Based on the process involved, these different approaches can be divided into two major categories; *"grow-in-place"* and *"solution-based (nanotube ink)"*. The "grow-in-place" technique allows simultaneous synthesis and deposition of nanotubes with moderate to excellent control of alignment (depending on the substrate). Significant and substantial challenges remain in controlling the ratio of semiconducting to metallic carbon nanotubes (typically 2:1, not sufficient for high performance electronics), and in controlling the nanotube diameter and chirality. While a combination of substrate controlled alignment and deposition control leads to atomic alignment with good semiconductor to metal ratios ~ 10:1 in certain substrates [7], (recently reviewed for ultra-high performance devices in [2, 3]), the generalization of this technique to other substrates and its wafer scalability [8] has not yet been demonstrated.

In contrast, extensive progress has been made in post-growth purification of SWNTs, leading to the prospect of a manufacturing and purification technology capable of delivering mono-dispersed SWNTs in solution of all the same chirality, diameter, length, and also (hence) type (semiconducting vs. metallic). While such a goal is not yet demonstrated (progress was reviewed in [9, 10]), commercial and academic sources already are able to provide 99% semiconducting nanotube material [11]. It is the availability of this all-semiconducting nanotube material that has given rise to the prospect of a high performance semiconducting ink, with mobilities that rival or even exceed the best available commercial semiconducting inks (other than nanotube) [12] by orders of magnitude.

Carbon nanotube based semiconducting inks offer great promise for a variety of applications including flexible, transparent, and printed electronics and optics. A critical drawback of such

inks has been the presence of metallic nanotubes, which causes high mobility inks to suffer from poor on/off ratios, preventing their applications in a wide variety of commercial settings. Here is presented a comprehensive study of the relationship between mobility, density, and on/off ratios of solution-based, deposited semiconducting nanotube ink used as the channel in field effect transistors. A comprehensive spectrum of the density starting from less than 10 tubes.μm^{-2} to the high end of more than 100 tubes.μm^{-2} have been investigated [13]. These studies indicate a quantitative trend of decreasing on/off ratio with increasing density and mobility, starting with mobilities over 90 cm^2 / V-s (approaching that of p-type Si MOSFETs) but with on/off ratios ~ 10, and ending with on/off ratios $>10^5$ (appropriate for modern digital integrated circuits), but with mobilities ~ 1 cm^2 / V-s. For the first time, this study carefully maps the relationship between density, mobility, on/off ratio, and spectroscopically determined purity, which lays the foundation for and opens up a wide range of applications of semiconducting nanotube inks in printed electronics.

3.1.1. OVERVIEW

What sets the mobility of a random network of semiconducting nanotubes in relationship to individual nanotubes? Can the mobility be increased by increasing the density? How does this affect the on/off ratio and what are the physical processes that set limits on this scaling?

The most obvious reason that networks have lower mobilties than individual nantoubes is that tube-tube crossings limit current flow from source to drain if the channel length is longer than the nanotube length. Increasing the network density can increase the current (and hence potentially the mobility). However, the complexity of such a system, coupled with the presence of metallic nanotubes which can short circuit the device if the density exceeds the percolation

threshold, means that there is no general theory that explains quantitatively the relationship between mobility, density, and on/off ratio, so that phenomenological experimental approaches are necessary for progress in the field.

Although solution based processing techniques enable the use of presorted semi-enriched nanotubes, limitations are imposed due to the fact that it is almost impossible to get cost effective 100% pure semiconducting nanotubes in solution. Therefore, all semi-enriched solutions available in the market so far contain some amount of metallic nanotubes which may impact semiconducting device properties. Other physical effects include the type of surfactant used in the nanotube ink suspension, deposition process (e.g. spin-on, ink-jet printed, drop-drying, gravure), wafer treatment used prior to nanotube deposition, and nanotube modification chemistry after deposition.

Although it has been known that in general, the transconductance and on/off ratio of solution processed nanotube transistors is highly related to the density of the tubes in a solution containing a mixture of metallic and semiconducting tubes [14, 15], no such experimental studies have been performed on purified all-semiconducting nanotubes which also would include the control over a wide range of different densities and in detail the effect of each density point on the mobility and on/off ratio. Snow et al. showed a solution-based deposition of nanotubes on a polymeric substrate which suffers from low on/off ratio since they used the mixture of metallic and semiconducting nanotubes in their solution [14, 16]. Also, their study shows no control over the density and its effect on the mobility and on/off ratio of the device. In another study, Hu et al. also demonstrates the effect of 3 different density points only on the sheet resistance of nanotube networks using a novel filtration method while, same as previous works, they used the mixture of

metallic and semiconducting tubes and also the nanotubes were deposited merely on filtering membranes which are not the desired substrates for electronic applications [17]. Other similar works show different deposition methods to have dense and aligned nanotube networks while they as well use the mixture solution of nanotubes and utilize a spin-on method that is not compatible with printed electronics [18-22]. However, none of these research studies were able to demonstrate a systematic study on density control to find the extremes for different applications. Furthermore, they use the mixture of metallic and semiconducting nanotubes in the solution as the base material. Recently there have been interesting investigations on purified all-semiconducting nanotube inks deposited on the substrate for fabrication of CNTFETs [23, 24].

So far, a systematic study of the relationship between the mobility, density, and on/off ratio of SWNT based semiconducting inks has not been reported, especially for the extreme limits on density at the high and low end. These are the key technical factors (in addition to cost, which is not addressed here) in determining if and when semiconducting nanotube based inks will ever find commercial applications. Figure 3.1 shows the sequence of parameters involved in defining the roadmap for nanotube based printed electronics.

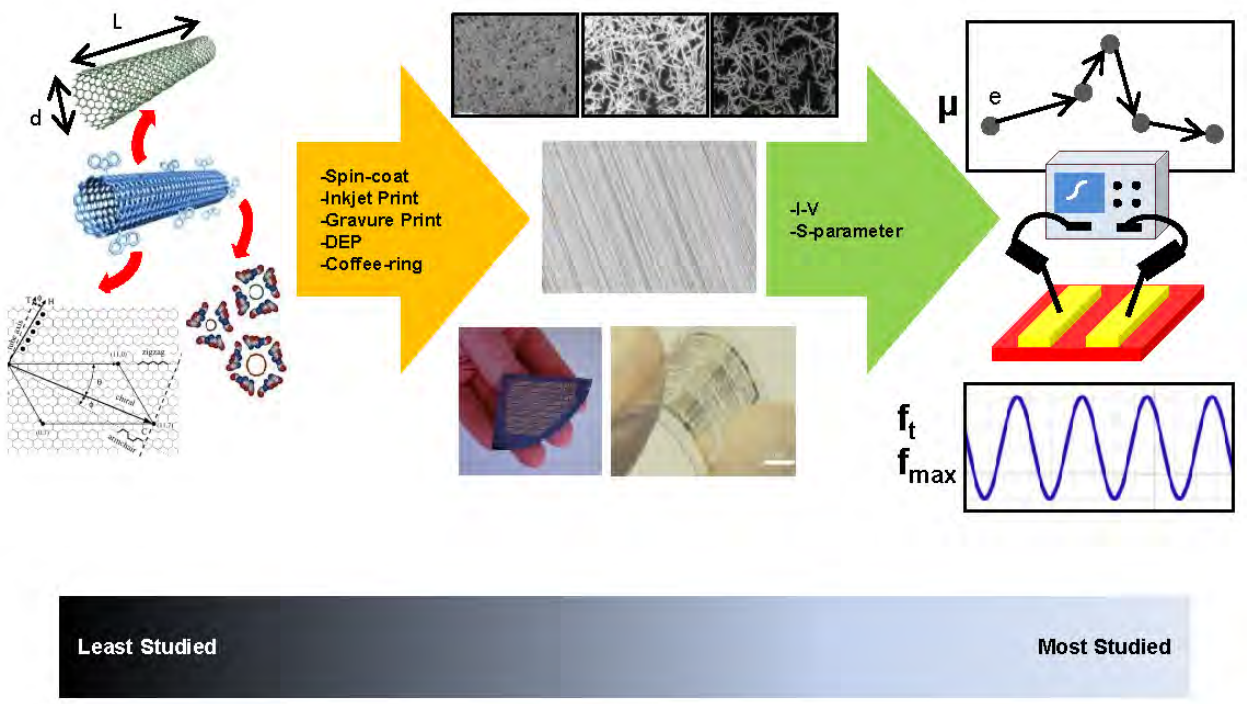

Figure 3.1. Overview of the carbon nanotube-based electronics process from the base material to device-level application [3]: ink chemistry and purification (left)[1, 9, 25], nanotube network deposition and formation (middle)[8, 13, 26], and electrical properties of the devices including "mobility", "on/off ratio", and "cut-off frequency" (right).

3.1.2. NANOTUBE SYNTHESIS AND PURIFICATION

The starting material for nanotube based inks can be synthesized with a variety of techniques. The most popular are chemical vapor deposition (CVD) and laser ablation. Generally speaking, these techniques involve a gaseous hydrocarbon feedstock at elevated temperatures, interacting with a catalytic nanoparticle. Typically, the average SWNT diameter can be controlled with some success [27-30], but the chirality is more difficult to control during synthesis. In the case of completely random chirality (which is typical for most synthesis methods), the resulting distribution of SWNTs contains a heterogeneous mixture of semiconducting and metallic SWNTs, with a mixture of 2/3 semiconducting and 1/3 metallic. This presents a severe problem

for nanotube electronics, as the metallic nanotubes can short the semiconducting ones in the case of a random mat of the material. Some progress has been achieved in controlling chirality during the growth [31-33] although challenges remain. For example, some work has shown a predominance of (6,5) nanotubes (over 50% in some cases) [32]. In general for small diameter SWNTs, if the diameter control is reasonable, then the number of possible chiralities is only a handful. However, for larger diameter nanotubes, the available (n,m) indices for a specific diameter are much larger (in the dozens), increasing the challenge of controlling the fraction of nanotubes of a specific chirality in the as-grown material. While it is clear that a large nanotube diameter is important for the development of low resistance metal-nanotube contacts [34, 35], its role in the properties of semiconducting ink is unclear. Therefore, there seem to be significant challenges in synthesizing SWNTs of the same chirality in the near future and it is unclear what routes will be able to achieve this. Although speculative, one long-term route would use synthetic bilogy to be develop an alternative, enzymatic synthesis process (a so-called "nanotube synthase" [36]), mimicking the atomic precision of biology. The prospect of this is quite long term, and difficult to achieve. One does not even know where to start.

Because of the daunting synthesis challenges, it seems that the most likely development of near term practical applications is the use of post-growth purification technologies. By and large, these have had extraordinary progress in the last 5 years, with a variety of techniques showing varying degrees of success in taking raw, as grown SWNT material and converting it into highly refined, purified solutions of in lab experiments of SWNTs of a specific diameter and chirality [9, 10]. Already commercial sources of purified semiconducting nanotube material are available for laboratory based experiments. Therefore, the development of nanotube semiconducting inks is a realistic and feasible prospect for a variety of technological applications in electronics.

Purification technologies fall into a couple of categories: flow based sorting (chromatography and electrophoresis/gel based methods), and density-gradient ultracentrifugation (DGU) [25]. The centrifugation sorting has been shown to allow separation of metallic from semiconducting nanotubes, based on differences in their buoyancy in response to different surfactants and functionalization chemistries in differing solvents [9, 10]. A variety of surfactants have been explored for this application, and the state of the art allows for reproducible 99% semiconducting solutions to be prepared. This seems the most logical starting point for nanotube based semiconducting inks, and is the most studied and understood to date. The issue of cost and yield for this technique still needs to be addressed, especially as it is a batch process. A complementary purification technique relies broadly speaking on flow based sorting techniques. This can be in the form of chromatography or gel and/or field based sorting. Chromatographic techniques have the potential advantages of continuous flow process, which may be lower cost, although this has not yet been determined.

These techniques have been shown to be capable of separating nanotubes not only on by their type (semiconducting vs. metallic) and diameter, but even on their chirality. Specific (n,m) indices can be extracted from a heterogeneous population. The process relies in many cases on preferential binding of specific chemical moieties to specific (n,m) indices. While a variety of binding moieties can be imagined, designed de novo, and tested, it is an even more exciting prospect to use known chemistry and analytical techniques of molecular biology to sort based on DNA [37]. Recent work [38, 39] has shown that DNA can bind with specific affinity to specific SWNTs, in a way that depends both on the base pair sequence and SWNT (n,m) index. Length based sorting using DNA is also possible, allowing study of nanotube length on electrical properties of networks [40]. Recently [41], our group assayed the binding of amino acids to

SWNTs, screening all of them, and finding SWNT specific amino acids that bind with specific affinity to SWNTs, with tryptophan the strongest binder. (This was verified by a different technique in [42].) There, we proposed to find or design peptide motifs with specific affinity to SWNTs of specific (n,m) index. This was actually carried out recently through a massively parallel bioinformatics screen of the entire protein data bank (PDB) followed by assays of a select subset of candidate motifs [43]. Thus, given the rapid pace of progress, it seems feasible that sorting technology will soon advance to the next level, and that purified solutions of SWNTs of a specific (n,m) index (rather than just a specific type) will be available at a commercial scale for prototype development. This will open a new window for studies and demonstrations of monodisperse SWNT solutions. Such a material would have tailorable properties for a variety of applications.

The challenge, then, is economical sorting. However, once that is solved, there is still a much bigger issue of deposition and electronic properties of SWNT networks post deposition, which is the main purpose of the project presented in this chapter.

3.2. OVERVIEW OF DEPOSITION TECHNOLOGIES

The prior section focused on theory of network electrical properties. Here is presented the various techniques that have been developed to deposit such networks. I first discuss the barest of inks, unpurified inks. Next, I discuss deposition of purified inks. Alignment techniques and purification techniques during and post deposition are then reviewed. While the techniques are listed separately for clarity of exposition, in practice many researchers demonstrate simultaneous

application of more than one of the techniques discussed below in an attempt to improve overall performance [3].

3.2.1. AS-GROWN NANOTUBE INKS

By far the simplest deposition technique involves deposition using ink jet or gravure printing techniques (Figure 3.2a,b), which result in completely randomly aligned nanotube networks. These techniques have the highest potential application in printed electronics, as they are extremely versatile and well developed industries, with very high production capacity once the ink is provided. Heterogeneous integration on virtually any substrate is possible. Ink development for printed circuits requires a variety of sources (metal traces, dielectric insulator, semiconducting channel), and my project focuses on the use of carbon nanotubes for the semiconducting ink. By using various ink solutions, a variety of resultant electrical semiconducting material properties can be achieved.

The simplest inks consist of as-grown nanotubes, which (as discussed) typically consist of roughly 30% metallic tubes. This technique (first pioneered by Snow, et al. [44, 45]) demonstrated mobilities of order 10-100 cm^2 / V-s, with on/off ratios of order 10-100. This technique has been reproduced by many labs around the world, and forms a robust, fundamental semiconducting material from simple principles [3, 22, 45-50]. However, due to the presence of metallic nanotubes, the on/off ratio is a challenge and has been given extensive attention, with attempts made to adjust the metallic nanotube density to be below the percolation threshold so that, in the off condition, the network is insulating.

While wet chemistry inks are the most versatile, a corresponding school of thought uses dry processing techniques such as vacuum filtration and stamping ("transfer printing"), which can result in similar networks of nanotubes. This is an alternative deposition technology with less flexibility in printing but more flexibility in integrating nanotube growth with the final network [17, 18, 26, 51].

3.2.1.1. Purification during deposition

Amine-terminated surfaces have been shown to aid in nanotube adsorption [52, 53]. It has also been known for quite some time that amine moieties selectively bind to semiconducting nanotubes over metallic varieties [54]. This concept can be exploited to achieve a quasi-purification effect while nanotubes are being deposited on APTES functionalized surfaces [13, 24, 49]. The resultant on/off ratio can be dramatically improved over and above that of unpurified nanotube networks, typically from ~10^3 to 10^6, using this technique alone. Mobility degradation does not seem to be an issue with this pre-treatment technique. Investigations of various surface chemistries provides an opportunity for engineering of the electrical properties, with modest control of network mobility by the surface treatment recently demonstrated [55]. However, it is fair to say that a comprehensive understanding of the effects of substrate material and surface chemistry on network properties is still a topic for future research, although to date (surprisingly), its effect seems to be rather modest.

3.2.1.2. Post-deposition purification

Several techniques exist to remove metallic nanotubes post-deposition. Early attempts at purification included electrical break down of metallic nanotubes. Collins *et al.* from IBM utilized electrical breakdown method to actually burn most of the metallic tubes in the channel

[56]. In their work they fabricate devices from as-grown nanotubes. By applying an appropriate gate voltage, the semiconducting nanotubes can be gated off so that electrical burnout only destroys the metallic nanotubes. A potential drawback of this method is scalability as well as control over the process, although work by Motorola and Stanford has shown interesting reproducibility in this area [57, 58]. It should be noted that, while the on/off ratio is improved, there is usually a reduction in the on current as well, sometimes over two orders of magnitude. The University of Central Florida has extended these studies in combination with dielectrophoresis (discussed below in the alignment section) [59-61].

Another approach consists of wet etching of metallic tubes. Generally speaking, this approach is based on the increased chemical reactivity of metallic nanotubes over semiconducting nanotubes, due to the increased density of electrons at the Fermi energy available for reaction chemistries (reviewed recently in [9, 10]). One of the early functionalization reagents used was diazonium to selectively react with metallic tubes [62-64]. Using a controlled concentration of diazonium, it is possible to suppress the metallic nanotubes suspended in solution [62] or after depositing them and fabricating TFTs [63]. An on/off ratio of 10^5 was obtained using this method [63]. Preferential metallic nanotube etching was achieved using a fluorine based gas-phase reaction [65]. Following on this theme, additional reaction chemistries involve cycloaddition reactions of nanotubes with fluorinated polyolefins [46]. Electron withdrawing non-fluorinated olefin chemistry is also effective, via a 2-2 cycloaddition reaction [47].

3.2.1.3. Stripe Method

Cutting the random nanotube network into narrow-width strips was demonstrated recently [66, 67] as an alternative to disrupt the metallic pathways from one electrode to another. Using conventional lithography and ion-etching technique they are able to divide a channel of width W into thinner strips of width W_S along with the effective direction of charge transport. In this way, the metallic pathways through the channel will be discontinued along the etched regions, resulting in lower off current and higher on/off ratio. Although this technique will inversely affect the mobility, optimizing the strip width (W_S) can assist in maintaining the mobility.

3.2.2. PURIFIED NANOTUBE INKS

Building on the deposition of mixtures, recent progress in purification technologies has led to the possibility of up to 99% semiconducting nanotubes (as determined by optical spectroscopic techniques) in solution (reviewed in [9, 10]). This has led to the demonstration of dramatically improved on/off ratios for a given mobility, recently demonstrated by several research groups [13, 24, 68-73]. The effect of SWNT nanotube density can be and was systematically measured by us [13], which allows for the first time a controlled determination of the trade-off between all the electrical parameters in the material, to be discussed further below.

3.2.3. ALIGNMENT METHODS

It is generally the case that improving the alignment of the nanotubes in the network will provide some degree of improvement in the network mobility [74]. Motivated by this effect, researchers have developed several techniques to affect alignment during deposition. To date, improvement in the mobility due to alignment has been modest and difficult to quantitatively

assess, at the cost of extra processing. Whether this extra complication merits application in a commercial manufacturing environment remains to be seen.

By far the simplest method to align during deposition involves spin-coating (Figure 3.2d) [49]. In this technique, radial orientation of the nanotubes is achieved. The wafer is simply coated as it spins, using techniques that are standard with the semiconductor processing industry. A drawback of this approach is the necessity to design devices and circuits with current flowing only in the radial direction. Similar flow based alignment methods have been developed where the fluid flow direction can control the deposited nanotube alignment direction [20, 44].

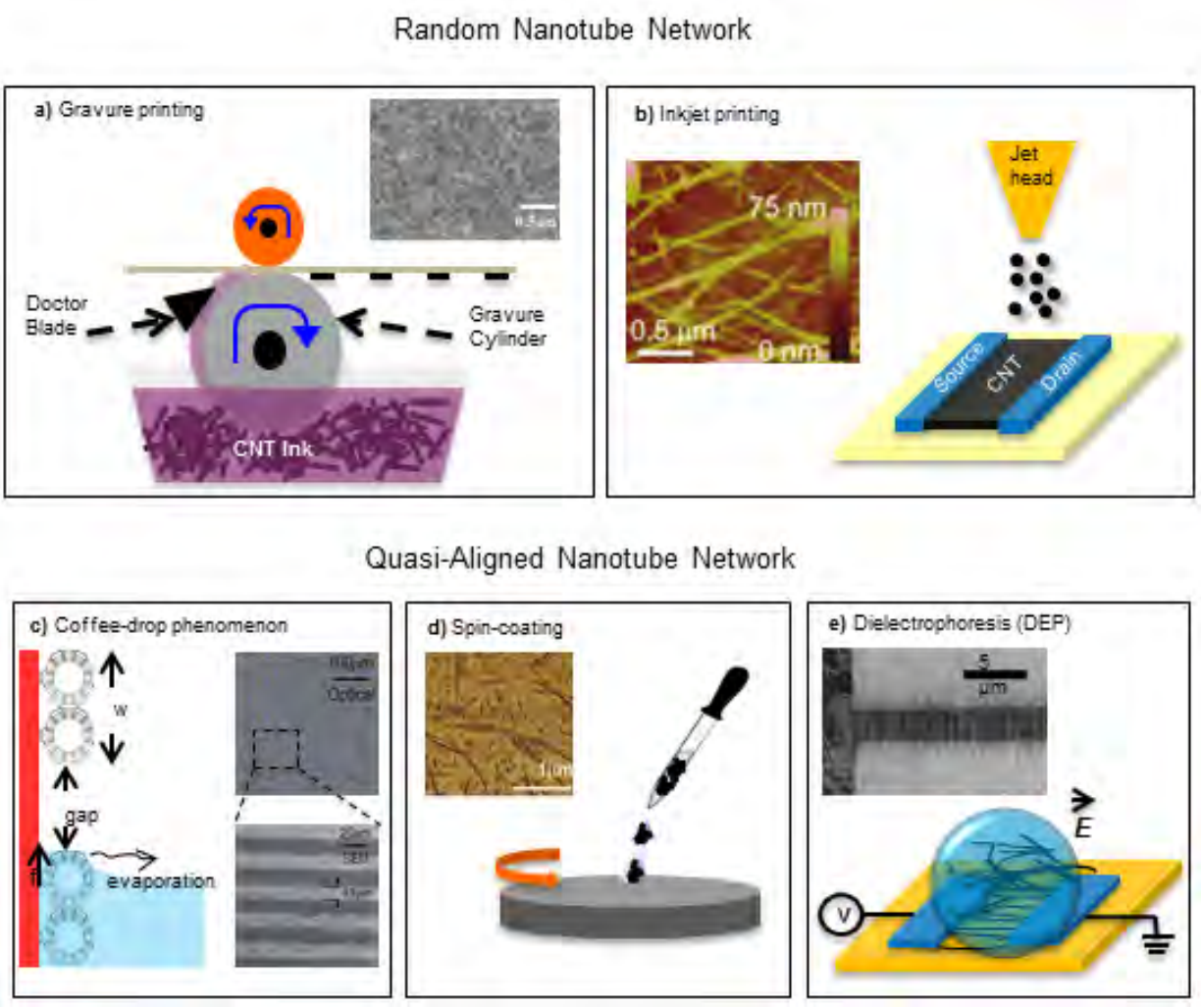

Figure 3.2. Deposition techniques [3]. Random deposition methods: a) Gravure printing using carbon nanotube ink [48]. b) Inkjet printing of nanotube ink [70]. Semi-aligned networks: c) Coffee-ring method using the surface friction for depositing nanotube strips [69]. d) Spin coating the nanotube ink resulting in radial alignment of nanotubes [46, 47]. e) Dielectrophoresis deposition which usually leads to preferential deposition of metallic tubes over semiconducting tubes [75, 76].

A more effective approach uses Langmuir-Blodgett troughs to achieve highly dense alignment [77]. A subtle related effect (Figure 3.2c) uses the "coffee-ring" phenomenon [78-81]. In this effect, as solvent evaporates, the nanotubes are deposited preferentially along the edge of

the bead of the solvent [69]. This allows alignment along the bead edge, which can be engineered to form aligned arrays of nanotube stripes.

A final alignment technology which has received extensive attention in the literature uses ac electric fields to align nanotubes during deposition as described in detail in chapter 2 (Figure 3.2e). The effect (dubbed dielectrophoresis (DEP)) is based on the time-averaged alignment force experience by a polarizable particle (or rod) in an ac electric field [59, 60, 75, 76, 82-85]. As discussed in the previous chapter, the voltage amplitude and frequency will determine the deposition result and the separation outcome. This technique (DEP) tends to result in preferential deposition of metallic nanotubes. In principle, engineering of the surfactant and ac frequency may allow this issue to be addressed [84] although in practice this has not been achieved.

One recent study [86] (also discussed later in this chapter) has shown that, with a starting purified solution of 99% semiconducting nanotubes, the resultant network, although highly aligned, can end up with mostly semiconducting nanotubes deposited (>97%) and good on/off ratio (varying from 1 to 10^3, depending on the density); mobilities are ~ 1-10 cm^2 / V-s. Another study [71] used ultra-high purity starting solution with trace amount of metallic nanotubes or less, and achieved high on/off ratio (10^5), and a high degree of alignment, albeit without excellent mobility (2 cm^2 / V-s). Thus, it seems DEP alignment of all semiconducting nanotubes is feasible, although (to date) the mobilities are one to an order of magnitude below randomly aligned but purified inks [13], indicating the relationship between alignment, mobility, and deposition process is not entirely understood. This could be because of the shorter source-drain spacing used in DEP based experiments, which tends to (but doesn't always) result in lower measured mobilities (Figure 3.10b).

3.3. THEORETICAL BACKGROUND OF NANOTUBE NETWORKS

The wide variety of parameters affecting the performance of nanotube networks makes it difficult to explore the response of such devices based on computer aided simulation tools. Among these parameters are the length and diameter of nanotubes, chirality and electrical characteristic of each tube (semiconducting or metallic purity percentage of the network), channel length and width, electrode contact resistances, tube-tube junctions, alignment degree (if applicable), and network density, which all should be considered to predict the functionality of printed devices made out of nanotube networks. For this reason, most progress to date has been based on phenomenological and experimental investigations of device performance. The following sections describe the predicted impact of the most important parameters on the ultimate electronic properties of nanotube networks, starting with the material properties, and ending with the system level performance. Here it is generally assumed that the channel length of the devices is longer than the average nanotube length (unless otherwise stated), i.e. longer than 1-5 μm. In this case, the network is a random network of metallic and semiconducting nanotubes, which must be modeled as such. This leads to scaling laws that differ from classical semiconductor MOSFET type devices, which will be expand upon.

3.3.1. PERCOLATION THEORY

3.3.1.1. Scaling with length

The most comprehensive model that exists is based on percolation theory, developed by Alam and colleagues at Purdue [66, 67, 74, 87-91]. The theory models the nanotube network as a random array of semiconducting and metallic nanotubes, with a fixed tube-tube conductance of

0.1 e^2/h. The metallic nanotubes are *on* all the time, and the semiconducting nanotubes can be gated on and off. This model explains a large quantity of data, although (as argued below), some significant anomalies remain. Reasons for this can include many effects that are difficult to incorporate into a simple model, such as tube-tube resistance, unknown distribution of nanotube chiralities and lengths in the network, effects of surfactants and functionalization on electronic properties, or the possibility of gating defects in metal SWNTs.

In this part, it's been reviewed a classical discussion of pure semiconducting nanotubes, postponing a discussion of metallic nanotubes to later. In a classical 2D conducting film, the ON current is inversely proportional to source-drain (or channel) length (L_{SD}). In a system close to percolation threshold, this is not the case. For densities near the percolation threshold, there are many nanotubes that are not involved in the current carrying process. These tubes form new percolating paths as L_{SD} reduces, and, therefore, the effective current increases faster with L_{SD} than the classical scaling law. For very high densities the classical scaling holds. This scaling law can be expressed quantitatively as:

$$I_{on} \sim \frac{1}{L_{CNT}} \left(\frac{L_{CNT}}{L_{SD}} \right)^{m} \quad (3.1)$$

Here L_{CNT} is the average nanotube length, L_{SD} is the channel length (source-drain spacing), and m is a universal constant which only depends on the normalized coverage (ρL_{CNT}^2, ρ corresponding to the density of nanotubes per unit area). For high-density networks, obviously, the network behaves like a classical conductor and $m \approx 1$. On the other hand, for densities near the percolation threshold, m approaches 2, and then diverges as the density approaches zero. For

moderate network density, *m* is typically between 1 and 2. Researchers have used fits to the power law to infer what region of percolation the device is operating in (near percolation, or very dense).

3.3.1.2. Definition and measurement of mobility

While classical percolation theory is applied typically in the linear response regimes (small source-drain voltages), important device operation occurs at large source-drain voltages. Alam [88] has generalized the theory for all regimes and has predicted the I-V curve should scale as:

$$I_{DS} = \mu_0 W C_{ox} \frac{1}{L_{CNT}} \left(\frac{L_{CNT}}{L_{SD}} \right)^m \left(V_{gs} - V_{th} \right)^2 , \quad (3.2)$$

where C_{ox} is the capacitance per unit area, V_{gs} the gate-source voltage, V_{th} the threshold voltage, W the width, and μ_0 the "mobility", to be discussed next. Note that Alam does not parameterize it this way, and only discusses the scaling law, not the prefactor, which is proposed here to interpret as follows: In the limit of very dense networks, well above the percolation threshold, the exponent m is 1, and hence the theory reduces to the classical theory, given by

$$I_{DS} = \mu_0 W C_{ox} \frac{1}{L_{SD}} \left(V_{gs} - V_{th} \right)^2 \quad (3.3)$$

Now is the time to consider the measurement and definition of mobility. In classical transistors, eq 3.3 holds for all conditions, so the mobility can be "measured" by using experimental values for dI_{ds}/dV_{gs} in the small signal (small source-drain voltage) limit as:

$$\mu_{"measured"} = \frac{\partial I_{DS}}{\partial V_{GS}} \frac{1}{V_{DS}} \frac{1}{C_{ox}} \frac{L_{SD}}{W} \quad (3.4)$$

or (in the large S-D voltage limit) by a fit to eq 3.3 (i.e. assuming that m=1 in eq 3.1). For classical semiconductor devices, both methods typically give the same result. However, in nanotube network devices, this is not always the case, so one must interpret the measurement of mobility with care. Almost all mobility calculations presented in the literature are based on the curve fitting to the *linear* region (low V_{DS}) but it is important to note that the actual operating region of the devices is in the *saturation* region.

In the high density limit (m=1), eq 3.2 reduces to eq 3.3, so the "measured" mobility (given by μ_0 from eq 3.2) can be interpreted as a classical, scale independent mobility. However, nearer to the percolation threshold, the "measured" mobility from eq. 3.4 is actually given by (using the parameters in eq. 3.2):

$$\mu_{"measured"} = \mu_0 \left(\frac{L_{CNT}}{L_{SD}} \right)^{m-1} \quad (3.5)$$

Thus, percolation theory predicts a "measured mobility" (which is what is quoted in the literature) would scale as ~ $1/L_{SD}$ in the percolation limit. This is actually NOT what is universally observed (see Figure 3.10b,), so the theory, while a good general framework, does not predict all of the scaling laws observed. In addition, eq 3.1 is obeyed in published scaling laws measured by Alam and collaborators [90, 91] and others [26, 45, 92, 93] on mixtures of metallic and semiconducting nanotubes, but not by all-semiconducting nanotube devices [3].

3.3.1.3. Capacitance

Individual carbon nanotube capacitance has been discussed in chapter 1 in details. It has been shown that carbon nanotube's capacitance consists of "*electrostatic*" and "*quantum*" components. Seemingly for the network of nanotubes the quantum component of capacitance does not change however, the electrostatic part should be reviewed. The capacitance coupling C_{ox} introduced in the following equation is also much different than that of classical thin-film materials. For nanotube-based transistors this capacitance mainly depends on the density of the network (separation between nanotubes), distance between the gate and the channel, diameter of the nanotubes, and the intrinsic quantum capacitance of nanotubes. A semi-quantitative model of the gate capacitance can be estimated for a network consisting of a parallel array of nanotubes with equal tube-tube distance [94]. An analytical expression of the gate capacitance based is given by

$$C = \{C_Q{}^{-1} + \frac{1}{2\pi\varepsilon_0\varepsilon_{ox}} \ln[\frac{\Lambda_0}{R\pi}\sinh(\frac{2\pi t_{ox}}{\Lambda_0})]\}^{-1}\Lambda_0{}^{-1} \quad (3.6)$$

where t_{ox} is the oxide thickness, and Λ_0 is the tube-tube separation, R is the tube radius, and C_Q is the quantum capacitance. As mentioned above, eq 3.6 is mainly used for aligned (parallel) network of nanotubes and therefore, for random arrays, it is expected to be a qualitative guide, but not to hold quantitatively. This capacitance modeling is significant in calculating the mobility of nanotube network films for different densities. Taking this capacitance into account, one can obtain more precise determination of the mobility.

3.3.1.4. Alignment

The network's alignment is an important parameter in defining the performance of the nanotube-based transistors. In general, for short channel devices (compared to the nanotube average length), better alignment yields higher current. However, for channel lengths much longer than the nanotube average length, perfect alignment in fact precludes any current flow at all. Therefore, there exists a practical optimum level of alignment, which depends in a complex way on the device geometry. In fact, for *long channel* nanotube transistors, a random network is in some cases close to being optimal [74]. Simulations show that the current is maximum at an alignment degree somewhere between perfectly aligned and perfectly random network of nanotubes. Indeed, for aligned networks, since the average tube length is much less than the channel length, the probability of individual nanotubes bridging from source to drain decreases drastically as the alignment degree increases. Thus, one only expects a modest performance improvement with increasing alignment.

3.3.1.5. On/Off Ratio

The on/off ratio is important in defining the power consumption of devices when used in digital circuits. In a mixture solution of nanotubes, the on current corresponds to both types (metallic and semiconducting) of tubes while only metallic tubes are responsible for the off current. The model used by most researchers assumes that the on current scales with length as eq 3.1 above, with "m" the exponent corresponding to the total density of the nanotube network (both the metallic and semiconducting nanotubes). In the off state, eq 3.1 still applies, but only for the metallic density, so that the exponent "m" is different. (Recall that m depends on the network density, as density increases m becomes closer to 1 (classical conductor) while for low density (near percolation), m approaches 2.) These two differing exponents (corresponding to the

two different densities) are labeled as m_{on} and m_{off}. Since the on and off current scale differently with channel length, these percolation models predict that the on/off ratio (R) scales as

$$R \sim \left(\frac{1}{L_{SD}} \right)^{m_{on} - m_{off}} \qquad (3.7)$$

with $m_{on} < m_{off}$. Therefore, the on/off ratio exponentially (m_{on}-m_{off}) increases as a function of L_{SD}. This model seems to describe much data of random mixtures of semiconducting and metallic nanotubes as well as purified nanotube inks [90]. Similarly, in purified networks $m_{on} < m_{off}$ but with much more difference between m_{on} and m_{off} (i.e. $m_{off} - m_{on}$ is bigger in this case), since the density of metallic nanotubes is small, the difference between on and off scaling exponents are even more and it is predicted that the on/off ratio should depend more on the channel length. However for sparse (low density) purified networks, $m_{on} \approx m_{off}$ and this dependence on channel length is predicted to be low/moderate.

3.3.2. FUNDAMENTAL LIMITS

In general, it is known that the mobility of an individual, pristine semiconducting nanotube (even for individual nanotubes deposited from solution) can be up to 10,000 cm^2 / V-s (depending on the diameter) [95, 96]. It should be noted that this mobility is achieved with nanotubes long enough to bridge the entire distance from source to drain. However, mobilities for random networks of carbon nanotubes (the focus of this project) have hovered until recently around the 1 cm^2 / V-s limit [2, 97]. Figure 3.3 shows the state-of-the-art limits for mobility and on/off ratio for different techniques.

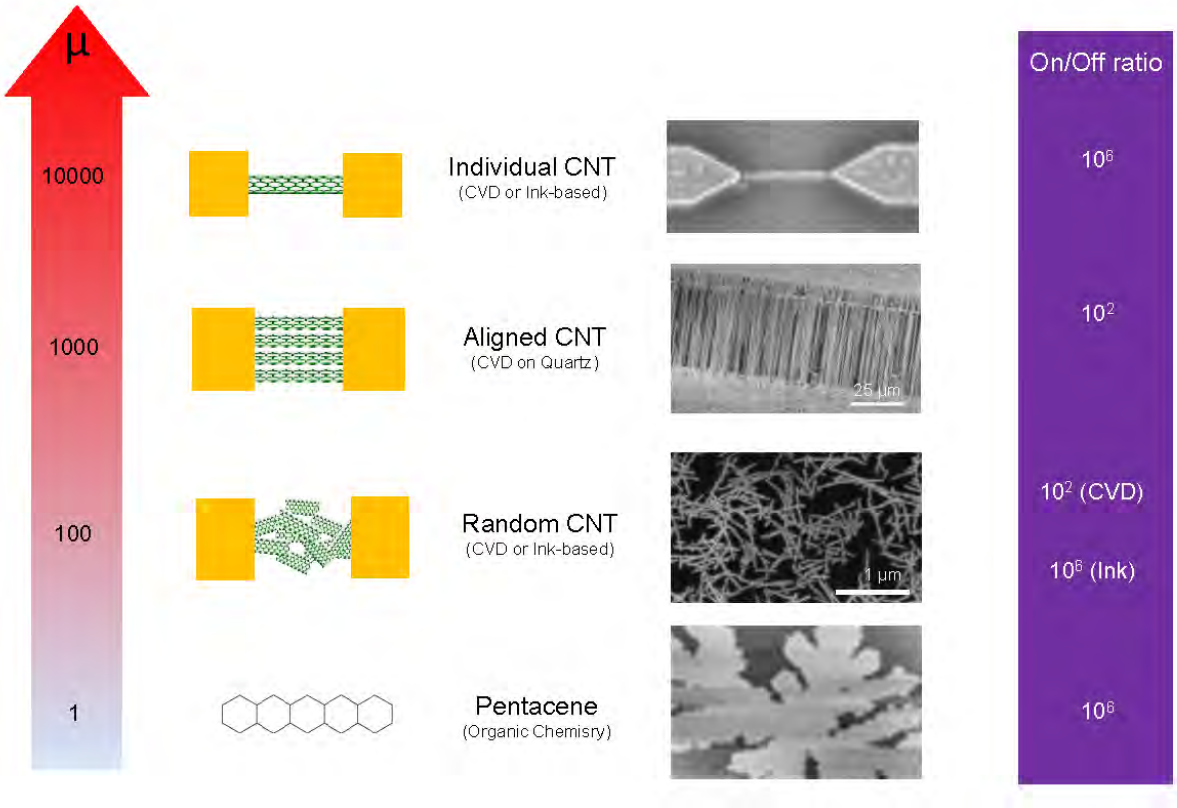

Figure 3.3. Mobility and on/off ratio trend and comparison between different techniques for nano-transistors [3]. From top to bottom: Individual nanotubes show the highest mobility but are not scalable yet [96]. Aligned SWNTs have low on/off ratio [75]. Random networks are scalable, high on/off ratio with moderate mobility and also the advantage of operating in the saturation regime as desired for field effect transistors [13]. Organic materials are alternative options with salability and on/off ratio but the state-of-the-art mobility is orders of magnitude lower than SWNT materials. The scale bar on the left shows the direction for increasing the mobility depending on the technique [12].

What sets the mobility of a random network of semiconducting nanotubes in relationship to individual nanotubes? Can mobility be increased by increasing the density? How does this affect the on/off ratio and what are the physical processes that set limits on this scaling? At the moment, no general theory exists which can answer these simple, but important, questions. Thus, even the simplest introductory question: (*What is the performance limit of semiconducting nanotube inks?*) has not yet been answered quantitatively from first principles. This motivates a

phenomological approach, and is the primary motivation for me investigating in this field. It is my hope that this will serve as a roadmap for the semiconductor industry as the technology gradually develops and moves from lab prototypes to commercial production.

3.3.3. SYSTEM PROPERTIES: FREQUENCY RESPONSE

Device mobility sets the current carrying capability and cutoff frequency. In long channel devices, cut-off frequency is proportional to the mobility of the device [2, 3, 98]. The relationship between mobility and cut-off frequency in *long channel* devices is described as

$$f_t = \frac{\mu\left(V_{gs} - V_{th}\right)}{2\pi L_{SD}^2} \quad (3.8)$$

where f_t is the cut-off frequency, μ represents the mobility of the device, V_{gs} ,V_{th} , and L_{SD} are as defined above. Note that for short channel devices (which are not yet applicable in printed electronics) the cut-off frequency only depends on the electron drift velocity (saturation velocity) and is inversely related to L_g. According to eq 3.8, it is advantageous to fabricate devices with very high mobility and short channel (gate) length. In radio frequency applications, power gain is also a critical figure of merit. An approximation of the frequency at which the power gain drops to unity (0 dB) is:

$$f_{\max} \approx \frac{f_t}{2[g_d(R_{ps} + R_g) + 2\pi f_t C_{pgd} R_g]^{\frac{1}{2}}} \quad (3.9)$$

where g_d is the drain conductance (dI_{ds}/dV_{ds}), R_{ps} and R_g are parasitic source and the gate resistances respectively, and C_{pgd} is the parasitic gate-drain capacitance [2, 3]. As known, the presence of metallic nanotubes results in non-zero $g_{d,}$, which reduces f_{max}. Therefore the capability of depositing purified semiconducting nanotube networks is essential for RF applications, even more important than the mobility or on/off ratio, which are easier to model and measure, and so more often discussed in the literature. Although both f_{max} and f_t are generally comparable in materials and devices with low g_d, they can be different by a factor of up to 100 in mixed SWNT networks [99] and even graphene [100]. Therefore, for practical applications, purified SWNT networks can have superior circuit performance even if the mobility is not as high as dense aligned arrays of SWNTs [101] or even graphene [100]. Recent work [102, 103] has achieved f_T, f_{Max} of 1-10 GHz using random networks of either purified or unpurified nanotubes, comparable to the best f_T, f_{Max} of dense aligned arrays [104] and graphene [100].

3.4. DEVICE FABRICATION

3.4.1. NANOTUBE DEPOSITION

Prior to the deposition of nanotubes, silicon substrates with 300 nm oxide layers (Si/SiO_2) were modified by 3-Aminopropyltriethoxy Silane (APTES) to form amine terminated self-assembled monolayers (SAM). In order to achieve these monolayers, wafers with oxide layers were first treated with piranha solution for 30-60 minutes at ~110 °C. Piranha-treated wafers were then thoroughly washed with DI water and dried by blowing compressed air. APTES solutions of 1% ~ 10% concentrations were prepared: 1 (or 10) mL APTES dissolved in 99 (or

90) mL isopropanol alcohol (IPA). Piranha-cleaned wafers were then dipped into APTES solution and left for 1 hour for surface functionalization. Wafers were then thoroughly washed with isopropanol (NO DI-water) and air-blown dried. For having different amount of modifications i.e. to have several different adsorption densities we used three different concentrations (1, 2 and 10%) of APTES solution in isopropanol. Using the higher concentration (>10% in isopropanol) resulted wafers with uneven surfaces that were not suitable for the device fabrications. Using 1% or 2% solutions yielded much more uniform nanotube network densities.

A semi-enriched solution (90% or 99%) was used to deposit SWCNTs onto APTES modified wafers. Wafers were first masked with a PET film and Krypton tape to leave 1 cm^2 open blocks. 20 μL of nanotube solution was then placed in each block and left for adsorption for 1 hour. Excess nanotube solution was then washed with DI water and wafers were air-blown dried. To achieve several different densities of nanotubes, we used three different concentrations (0.005, 0.01 and 0.1 mg/mL) of nanotube solution. Each solution was used for the deposition on APTES modified wafers having different adsorption densities.

Solution-processed separations of nanotubes generally involve the use of surfactants to solubilize raw nanotube mixtures in DI water or other solvents before further processing. The concentration of nanotube dispersions highly depends on the surfactant used. For the most widely used surfactant sodium dodecyl sulfate (SDS), the maximum concentration is reported to be around 0.12 mg/mL [105], although when these solutions are further processed for purification and separation, only a fraction of nanotubes compared to the starting solution are left in the resultant solution. In our experiments, we varied the nanotube concentration until just prior to precipitation, and also via dilution until no nanotubes were visibly deposited. When the

solution was diluted to 0.001 mg/mL, after deposition very few nanotubes were found on wafers for any amount of surface modification. On the other hand, increasing the concentration up to 0.1 mg/mL (by evaporative drying) resulted in precipitation of nanotubes from the dispersion. Using this method, a great control over the entire possible range of nanotube concentrations in the ink was achieved prior to deposition, in order to investigate their effects on the final mobility, network's density on the wafer, and on/off ratio. Different densities were obtained by diluting or evaporating the primary nanotube solution. Nanotube ink is received with the concentration of 0.01 mg/mL. To dilute the solution (gaining low densities) we added SDS (sodium-dodecyl-sulfate) to the as-received ink. SDS is prepared using 1.5 gr of SDS powder dissolved in 100 mL DI-water resulting in 1.5% (weight by volume) SDS solution. Next, the final solution was sonicated for ~30 minutes to disperse the nanotubes thoroughly in the solution and prevent the formation of bundles. In contrast, to make denser tubes two methods used. In first method we dried out the solution, monitoring the level of liquid, until it reaches the preferred point. This is not an accurate way of changing the density. The second and better approach was to dry out the solution completely and then again add the SDS solution to the remaining (which is only the nanotubes). After adding SDS the sample was sonicated for ~30 minutes. It should be note that every time something added to the nanotube ink, the solution should be sonicated for at least 20-30 minutes to ensure the uniform dispersion of nanotubes. Besides, if the nanotube ink is left on the shelf for some time, it is recommended to sonicate the solution to break any possible nanotube bundles.

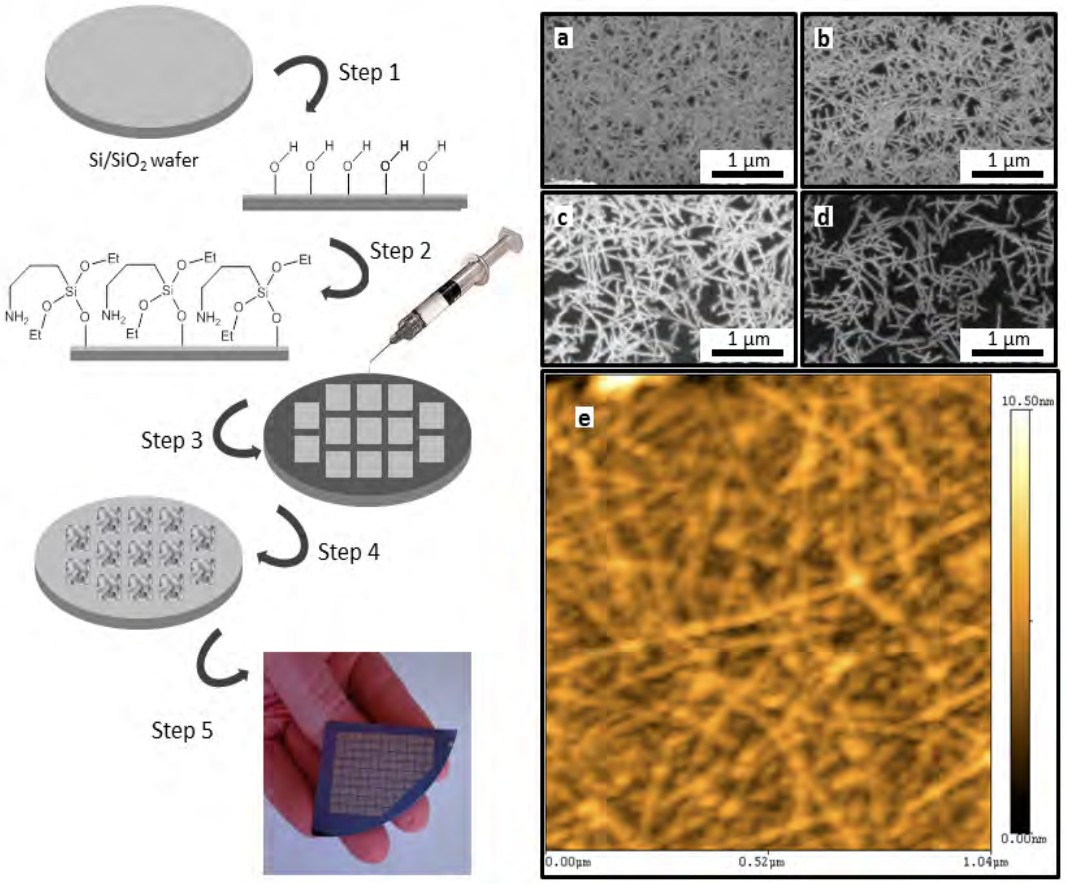

Figure 3.4. Deposition Protocol [13]: (On the left) A schematic diagram of all semiconducting nanotube device fabrication. SiO_2 coated Si wafer was first treated with warm piranha solution that introduces –OH groups to the oxide surface (step 1), wafers were then introduced to APTES/Isopropanol solution for surface modification (step 2) by self-assembled monolayer (SAM) of amine terminated silane (APTES), on these modified wafers 1 cm^2 blocks were created using a PET film mask with pre-cut 1 cm^2 blocks, 20 µL of semi-enriched nanotube solution was dropped into each of these blocks (step 3). Wafers were then air dried (step 4) prior to electrode deposition onto them (step 5). SEM Images (On the right) SEM images of devices having different densities of nanotubes, nanotubes count estimated by visual inspection of SEM images for each of these device are 85, 50, 25 and 10 per μm^2 for devices shown in a, b, c and d respectively. e) AFM image of nanotube network deposited on wafers.

In sum, to obtain a range of densities of nanotubes on wafers, we chose to vary two important factors related to the deposition process – (a) variations in the amount of surface modification by

using APTES/isopropanol solutions with different concentrations and (b) changing the solution concentration of nanotubes used for deposition. Keeping one factor same at a time and varying the other factor resulted devices with several different distributions of nanotubes. Based on visual inspection of SEM images obtained from different locations on each channel for every device, number of nanotubes was counted in a 1 μm^2 area of the image. Images taken at different locations for each channel show a very uniform nanotube-network channel. Tube densities (D) ranging from 10 to 100 tubes per μm^2 was deposited to investigate the impact of tube density on both the mobility and the on/off ratio. Figure 3.4 provides the deposition technique, SEM images of the deposited nanotubes with different densities, and AFM (Atomic Force Microscopy) of a nanotube network.

3.4.2. BACK-GATE DEVICES

Devices in a back gate configuration with channel lengths ranging from 10-100 μm (with 10 μm increments) were fabricated. 300 nm thermally grown high quality (chlorinated) dry oxide cap is used as the insulating layer for the back gate Si substrate. Low resistivity wafers (1-20 Ω-cm) were used as back-gate. In all the devices, the gate width is fixed at 200 μm. Here the SEM and schematic of back gate configuration of devices is demonstrated. Since one future goal of this project was to investigate the performance of these devices in radio frequency regime, the electrodes where fabricated in rf-compatible structure of ground-source-ground (GSG) fingers. Figure 3.5 demonstrates the devices design and schematic along with a sample SEM of deposited nanotube in the designated channel.

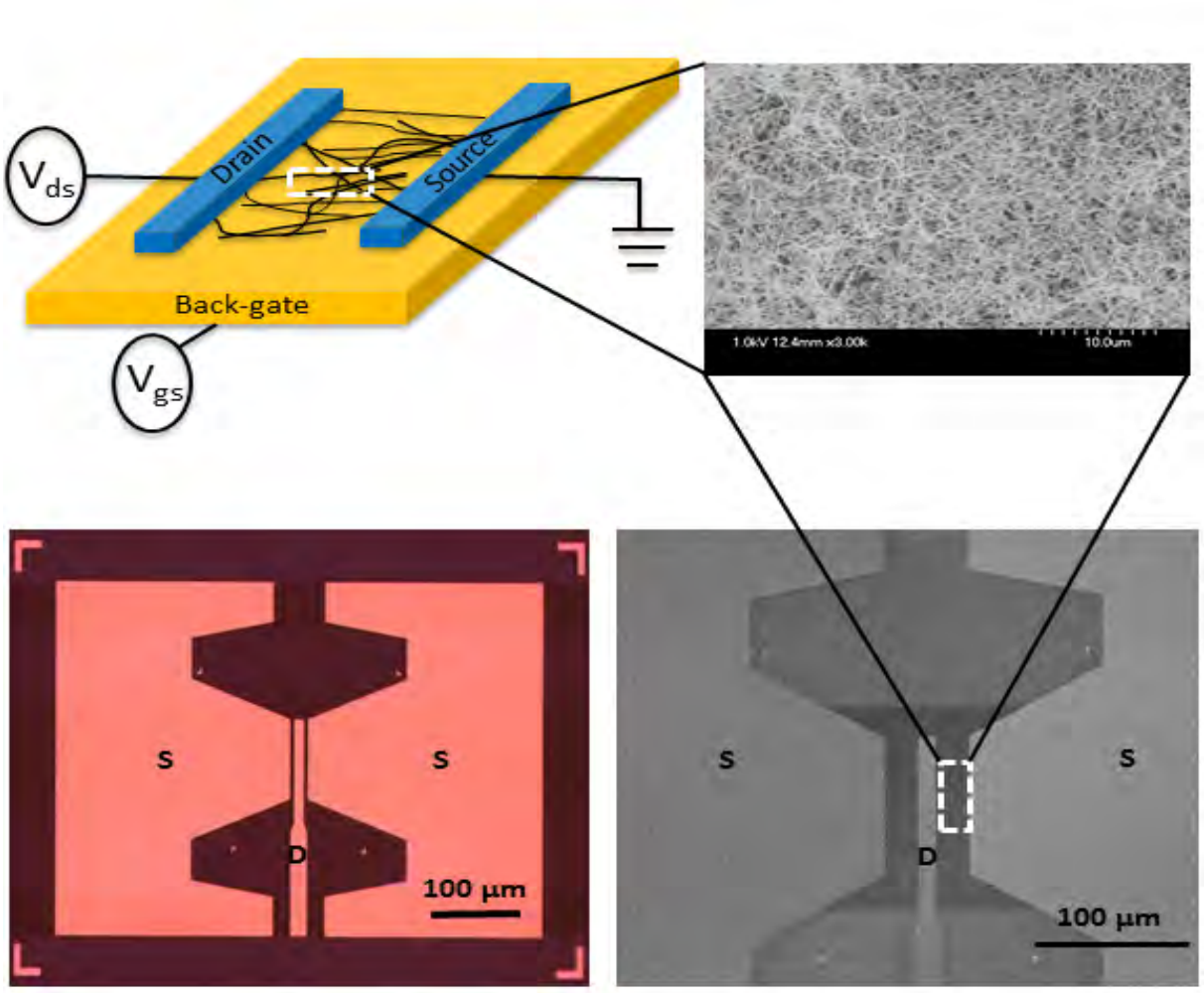

Figure 3.5. Device schematic, optical image, and SEM of the structure and nanotubes deposited in the channel (scale bar in SEM image is 10 µm).

Following the nanotube network deposition, photoresist (PR) was spun on the devices. Shipley 1827 (2.7 µm) was spun with 3500 rpm (560 initial acceleration) for 40 seconds. The PR thickness will be around 2.5 µm. Samples are then put in pre-bake oven (90 ^{o}C) for 20-30 minutes (~25 minutes) so that the unwanted solvents are evaporated. Using MA-6 Karl Suss mask aligner and designed mask, source and drain areas were shined at with UV light (~ 140 mJ). Subsequently, samples were immersed in MF-319 developer to pattern the source/drain

electrodes. Next, samples were put into e-beam evaporation system. 15 nm of Palladium (Pd) was first deposited with 0.1-0.5 A^o/sec rate followed by 30~100 nm of Gold (Au). Pd is known to make an ohmic contact with nanotube, therefore it is used as the first metal connecting to nanotubes. However, gold is very low resistance and chemically stable (no native oxide will form above gold metal) electrode which is commonly used for electrodes. Afterwards, samples are dipped into Acetone bath for lift-off the photoresist along with the unwanted metal. For devices with low channel length (10 μm and less), Shipley 1827 is not a proper photoresist to use. There is another technique which deposits high-resolution photoresist, called PMGI, as the first layer and then Shipley 1827 is deposited on top of that. This method is suitable for resolutions down to ~250 nm. Using PMGI however, slightly changes the method. Sample is first covered with PMGI (colorless) and left for 5-10 minutes (~6 minutes). Then we turn on the spinner (3500 rpm, 40-45 sec). Pre-bake is done on hot-plate (170-200 ^oC) for 5 minutes. After the PMGI deposition step in completed, Shipley 1827 (or 1808 based on the application and thickness required) is spin-coated using the conventional method mentioned above and sample is patterned (same power in MA-6) and developed (MF-319) same as Shipley PR. Another change in the method is the last step for lift-off process. After the e-beam evaporation deposition of metals, samples are dipped into Nano-Remover (PG) which is proper for PMGI. Note that Aceton bath SHOULD NOT be used at all for lifting-off the PMGI photoresist (using Acetone instead of Nano-remover will result in a milky solution and damages the devices). Samples are left in Nano-remover until the unwanted layers come off, then the second bath of Nano-remover is used for completely removing the PMGI (can be warmed up a little but not necessarily). Next, devices should be immersed into isopropanol alcohol (IPA) for about 10 minutes and then

washed with organic solvents (IPA, Methanol, or Acetone) and DI water. The fabrication steps are shown below.

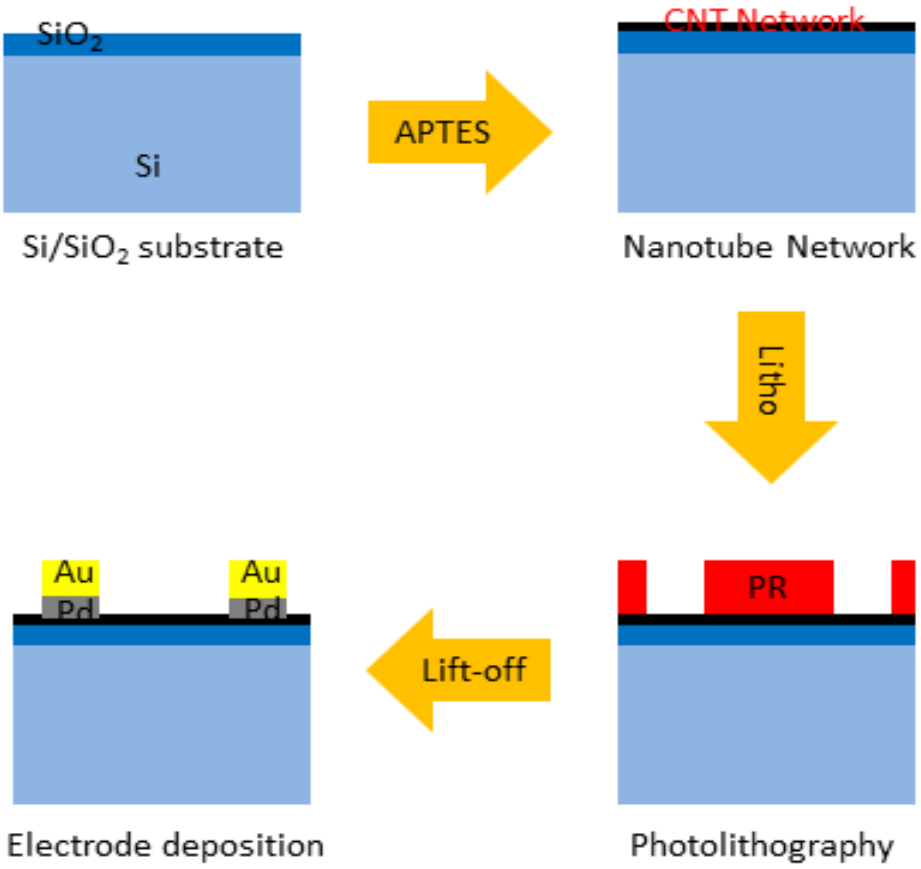

Figure 3.6. Schematic of fabrication process

3.4.3. ELECTRICAL MEASUREMENT RESULTS

Devices are now ready for measurement. The first basic measurement is to investigate the I_{DS}-V_{DS} characteristic of the device. . As shown in figure, the I_{DS}-V_{DS} curve is linear for V_{DS}

changing between 1 V and -1 V, indicating good ohmic contact between the nanotubes and the electrodes as a result of using Pd. By applying more negative V_{DS} the devices clearly show saturation behavior (Figure 3.7a). The devices exhibit p-type behavior, consistent with prior works on nanotube networks since nanotubes are considered to show p-type characteristic due to the absorption of oxygen (with high electron affinity). Gate voltages applied to these devices are ranging from -10 V to +10 V with source/drain voltage of 0 – 7 V.

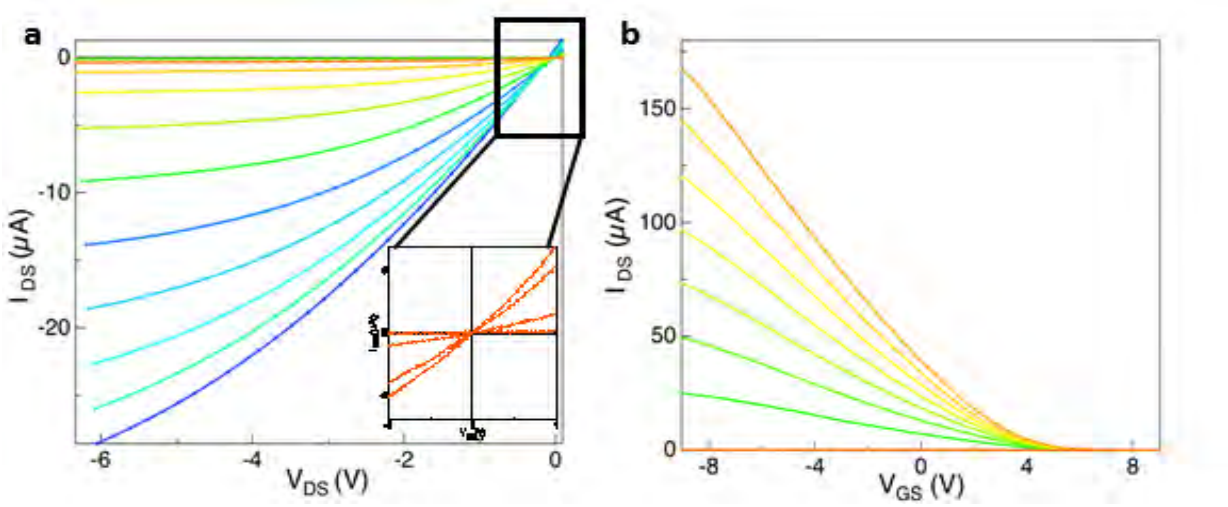

Figure 3.7. a) Current-voltage characteristic of a device with channel length of 100 µm and W = 200 µm for different gate voltages ranging from +10 V to -10 V in 2 V steps, showing the expected saturation behavior at negative gate voltages and high drain-source voltage (V_{DS} changes from 0 V to 6 V). b) Depletion curve (I_D-V_G) of a device with channel length of 100 µm and drain-source voltage changing from 0V to 7V.

3.4.3.1. Mobility and On/Off ratio

Using the conventional I-V equations for MOS devices as described in eq. 3.4 in triode region, we calculated the mobility using curve fitting to the experimental results (Igor Pro software was used). For calculation of the capacitance, we used eq. 3.6 with t_{ox}= 300 nm. With nanotube lengths in the range of 1~5 µm, and network densities of 10-100 nanotubes/µm^2, we expect that the parallel plate capacitance underestimates the actual capacitance by about 30% for

the lowest densities we use, and less so for the higher densities. Therefore, our use of the parallel plate capacitance (eq. 3.6) for estimating C_{ox} is justified.

Using this technique, we find our devices have mobilities ranging from 1-90 cm^2 / V-s (if we use eq. 3.6 for low density samples to estimate the capacitance). The highest mobility devices have in fact higher mobility than any published nanotube network device fabricated from purified (semi-enriched) SWNT devices, indicating that we are successfully probing the ultra-dense limit of SWNT devices.

Although the mobility should be a bulk property (independent of device length and width), because of the presence of metallic nanotubes and percolation effects, it has been commonly observed in as-grown nanotube networks (containing roughly 1/3 metallic and 2/3 semiconducting nanotubes) that the mobility does in fact depend on gate length as discussed above. In this work also length dependence to the mobility, on current, and transconductance was observed, as shown in Figure 3.8. The overall scaling with length does not depend strongly on the purity of nanotube starting material, as shown in Figure 3.8a.

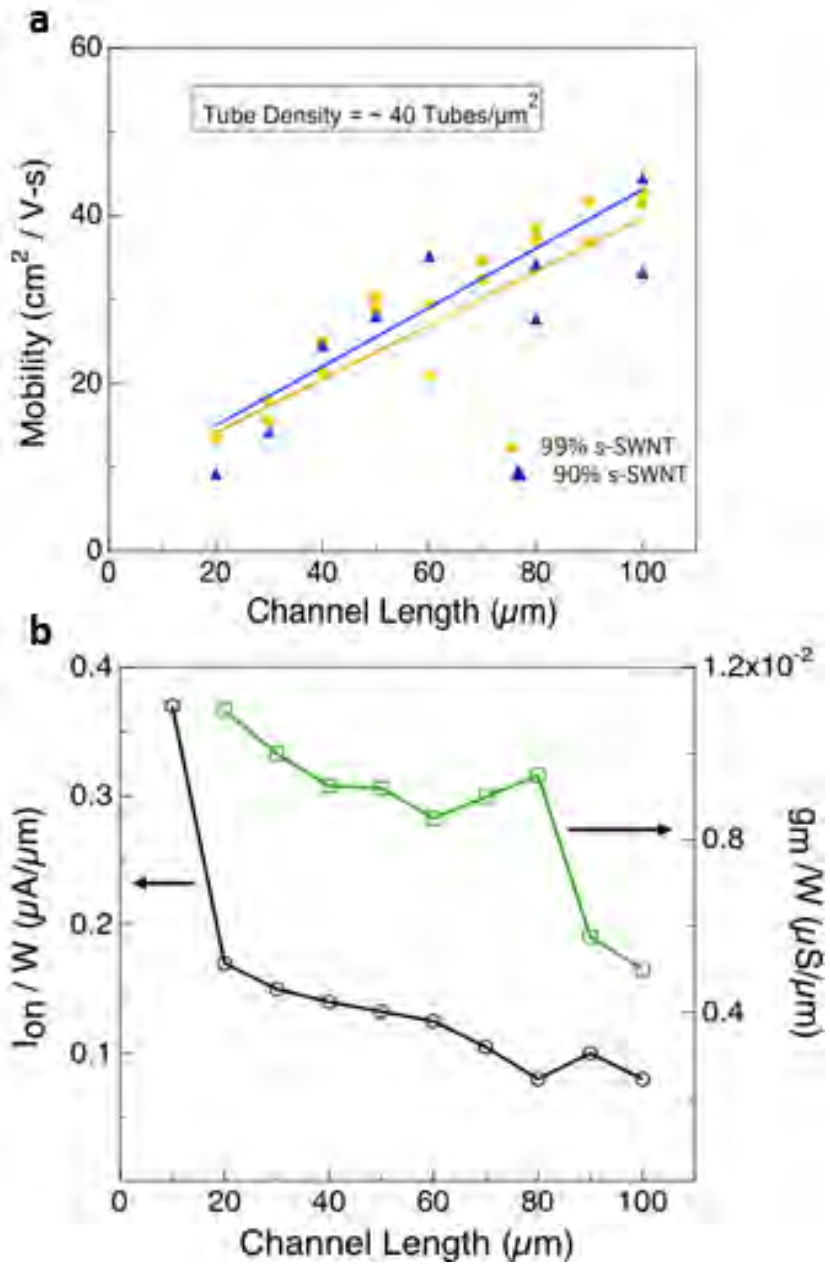

Figure 3.8. Channel length impact [13]. a) Mobility vs. channel length for $L_{channel}$ = 20 μm to 100 μm. As a sample, the measurements were performed on devices with the moderate tube density of around 40 tubes per μm^2 and for 2 different semiconducting to metallic ratios in the solution. Tube density was controlled both by the surface modification and the density in the solution. b) Current density vs. channel length (W is fixed at 200 μm) on the left axis shows a decrease in I_{on} as the channel length increases to 100 μm. The right axis demonstrates the transconductance per unit width (g_m/W) decreases by increasing the channel length.

Although the mobility for 90% semiconducting tubes is expected to be slightly higher (at a fix channel length) due to the presence of more metallic tubes, here we found no significant difference between the mobility of 90% versus 99% semiconducting ink batches. This can be explained with regard to the fact that the purity percentages of the batches are defined via spectroscopy techniques and not electrical measurements. Therefore, there is a good chance that the accuracy of the purity percentage is not always set to stone and varies from batch to batch using the same purification technique. Another concern is the contact resistance. Although we used Pd for contact, the nature of metal to nanotube network contact is yet not clear and it can be the cause for the length dependence of mobility as well (discussed more later).

The on/off ratio is more than 1000 in most of the devices, especially the ones with longer gate lengths, leading us to the conclusion that the surface treatment will also help us with the deposition of semiconducting tubes although the solution was 99% semiconducting enriched already. Study of the on/off ratio showed that 20 μm is a turning point for on/off ratio. For most of the devices with the gate length of more than 20 μm, the on/off ratio is more than 1000 while for smaller gate lengths this can come below 100 in some cases due to the presence of metallic nanotubes which correspond to metallic pathways between electrodes and increase the OFF current. The highest on/off ratio we observed was around 110,000.

3.4.3.2. Scaling with SWNT density

So far, the electrical characteristics and the improvement made to mobility and on/off ratio of the purified nanotube TFTs is presented. In this section the fundamental root of this variety in the output characteristics is discussed more in detail. As shown in the theoretical background, density of as-grown nanotubes plays an important role in final output behavior of nanotube

transistors. In this project for the first time we investigated the effect of nanotube network density deposited through ink, in the output characteristic of TFTs. The density variation technique was described in previous sections (deposition methods used here) and SEM images confirm variety of densities obtained in different devices.

Figure 3.9a plots the mobility vs. nanotube density. The only varying parameter was the tube density. Different nanotube densities were obtained by controlling the density in the solutions, as discussed earlier. This allows us to systematically evaluate the effect of nanotube density on mobility. It is clear from the plot that increasing density increases the mobility. While this is consistent with prior reports on random arrays of as-grown (1/3 metallic and 2/3 semiconducting tubes) and simulations of such systems [15, 24], this is the first systematic study of this effect on devices made of purified, all semiconducting nanotube ink.

On/off ratio is also one of the important figures of merit especially for digital switching and low power applications. Figure 3.9b shows the degradation in on/off ratio as the density of nanotube film increases owing to the fact that when the semiconducting nanotubes are all gated off, the background conduction of metallic nanotubes will depend in a non-trivial way on the density, due to percolation effects. Increasing overall density will increase metallic density which will increase the off current. Similarly, increasing overall density will increase the on current, due simply to the increased # of tubes. However, the effect of the density on the on/off ratio is much more difficult to predict theoretically.

In Figure 3.9c, we plot the mobility as a function of on/off ratio. For a given gate length, we observe a very clear trend of the on/off ratio with mobility, starting with mobilities over 90 cm^2 /

V-s (approaching that of p-type Si MOSFETs) but with on/off ratios ~10, and ending with on/off ratios $>10^5$ (appropriate for modern digital integrated circuits), but with mobilities ~10 cm^2 / V-s.

While simulations can attempt to reproduce the features, there is no substitute for a quantitative, systematic study of the effects of density on on/off ratio and mobility, which we have presented in Figure 3.9c.

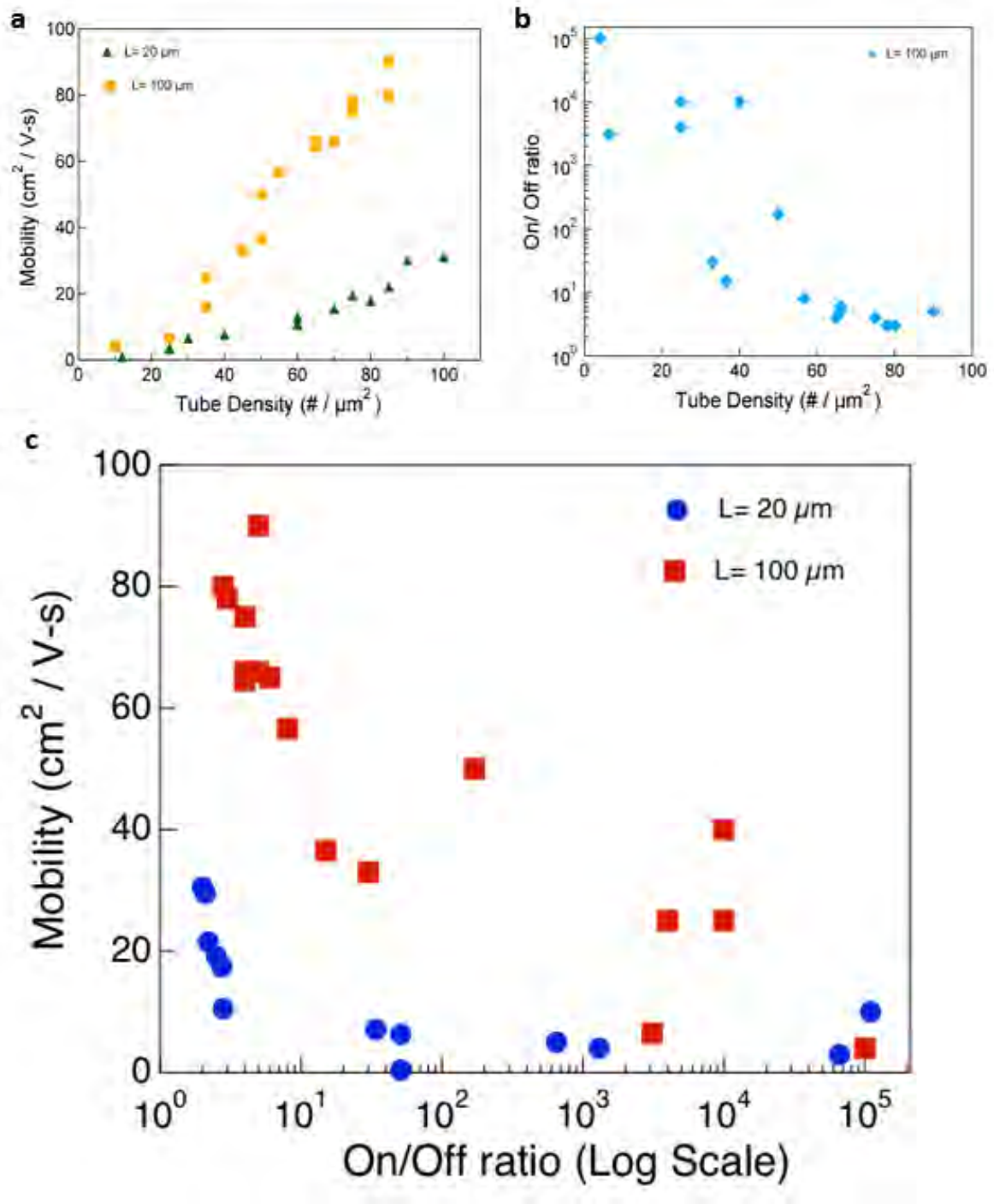

Figure 3.9. Mobility and on/off ratio. a) Mobility as a function of nanotube density for lower and upper channel length extremes ($L_{channel}$ = 20 μm and $L_{channel}$ = 100 μm). Mobilities of around 90 cm^2/V-s were achieved at the high-density limit of nanotube deposition and the channel length of 100 μm, and W = 200 μm. b) On/off ratio dependence on the nanotube network density for $L_{channel}$= 100μm. c) Mobility as a function of on/off ratio showing the inverse relationship for the same devices in a, b.

3.4.4. TOP-GATE DEVICES

So far we discovered many unknown aspects of nanotube ink based thin film transistors using back-gate structure. Another direction would be to try the top-gate configuration. One would expect the same results, however to date there is no clear study on the top-gate nanotube based transistors. The main issue is finding a suitable high-K dielectric that gives a complete coverage over the nanotubes and is compatible with the rest of the process especially when it comes to printed electronics (the dielectric should also be printable). In addition to that, the material used for top dielectric and process of depositing the dielectric may change the behavior of the device completely.

For this project, we tried different top gate dielectrics including SU8-2005 (a negative photoresist, bought from Microchem) and HfO_2. SU8 has the advantage of spinning-on process, flexibility, and ease of use as the top gate dielectric. However, in our application, since we require a very thin layer of SU8 (around 500 nm or less) the pinholes may introduce connection paths from the gate on the top to channel and source/drain electrodes. The spinning parameters are 500 rpm for 10 sec and 4000 rpm for 30 sec to get a uniform 460-500 nm thickness of SU8. The sample is then prebaked on top of hot plate (95 ^{o}C) for 1 minute. Using a proper pre-designed mask, the sample is exposed to UV for 10 sec (@ 6 mW/sec). Subsequently, the sample is post-baked on hot plate (95 ^{o}C) for 2 minutes and developed (using proper developer for SU8) for 1-2 min. Different curing and spinning processes have been studied but neither was successful in achieving a thin dielectric layer of only SU8 without gate leakage current.

The second choice was HfO_2 which can be deposited by the means of both e-beam evaporator and/or ALD (Atomic Layer Deposition) machine. Basically the devices were

including random network of nanotubes with source and drain electrodes on top, then HfO_2 was deposited on top of the whole device. We first used a thin layer (50 nm) of e-beam deposited HfO_2 from the HfO_2 pellets. Same as above, the pinholes in the thin layer of dielectric caused via paths from gate to the bottom electrodes and as a result, high gate leakage in the devices under bias.

Then ALD was used to deposit HfO_2 (20 nm) on top of the nanotubes network. The first sample had gold (Au) as the top metal in source and drain electrodes which does not seem to be an appropriate choice for ALD deposition of HfO_2, therefore we changed the electrodes to Nickel in second batch. The second batch of samples were also put in ALD but the process happened to have some complications such as photoresist residue from the lift-off step, although the devices were dipped in Acetone for a while before putting in ALD machine. After further investigations, EKC was found to be a proper solution for cleaning/removing the residue of the Shipley photoresist. Samples were dipped into hot EKC (@ 80 ^{o}C) for 5~7 minutes and then rinsed in isopropanol alcohol (IPA) for few minutes. Following the cleaning procedure, the 20 nm ALD was deposited. The results showed leakage current above the proper level for the device performance. This time the main reason is thought to be gate and source/drain overlap and/or the existence of pinholes in ALD HfO_2, right above the nanotube channel, because of the wet process used to deposit the oxide while carbon nanotubes are known to be hydrophobic. The gate leakage current is found to be around 20 μA for 3 V gate and the gate area in our electrode design. Taking all these results into account, we realized that exploring the top gate behavior of nanotube devices especially deposited through nanotube ink is not a solved problem yet and not the primary intention of this project as well. Talking to other experts around the world we

figured out that most of them (particularly the ones working with nanotube ink) are having the same issues with their top gate structures.

3.5. DISCUSSION

3.5.1. ROADMAP FOR APPLICATIONS: PHENOMENOLOGICAL NANOTUBE NETWORK ENGINEERING

Theoretical models were discussed earlier that show nanotube network properties as a function of materials parameters. Many of them are based on computational models, and some on physical assumptions that are hard to test. In addition, experimental methods were considered to study several unsolved issues in the field. Based on that, we argue that a phenomenological approach is required to establish the field of nanotube network engineering. Below is provided an overview summary of experimental work published to date (including our works), to establish trends, confirm models, and point out inconsistencies. Collectively, these observations lay a roadmap for future applications of nanotube semiconducting inks, including applications of existing technology, as well as avenues for potential improvements.

3.5.1.1. Scaling with device length

The mobility of a classical semiconductor is independent of its length. However, for nanotube networks, mobility is a more complex concept, as discussed in the theoretical section. In order to compare mobility from one device to another, the length of the device must be specified. As discussed in the introduction, the mobility according to the most sophisticated percolation based theory should be inversely proportional to length. However, in practice, this is

not always the case. . The length dependence is not purely an alignment effect. For example, Figure 3.10a shows the length dependence of aligned arrays, which is increasing with length (possibly due to contact resistance effects).

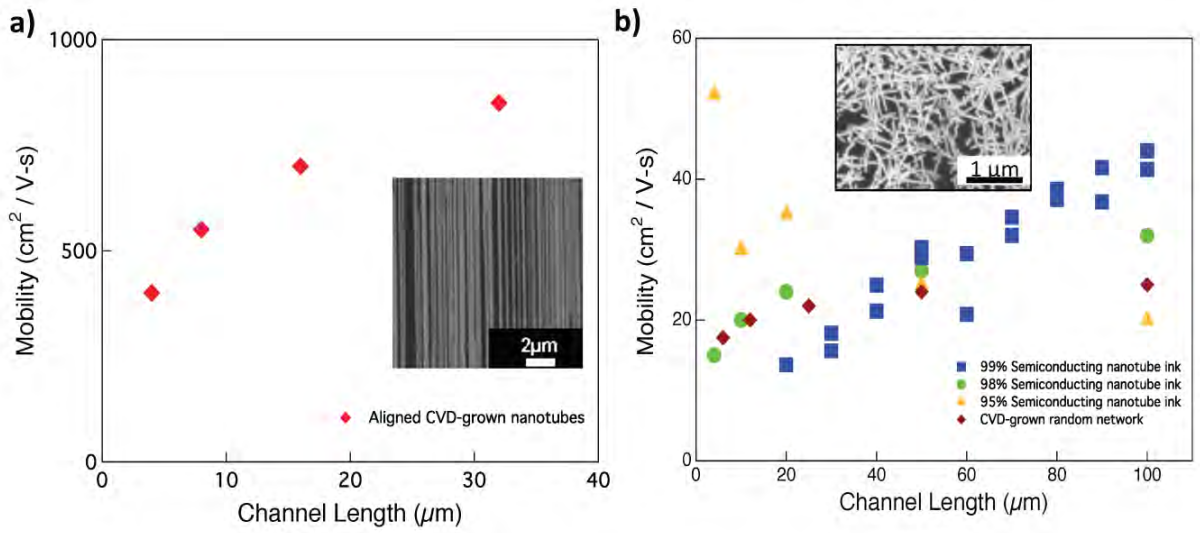

Figure 3.10. Mobility vs. channel length [3]. a) Mobility as a function of channel length for CVD-grown aligned nanotubes on quartz substrate. Mobility rises up as the channel length increases. High mobility is due to the high degree of alignment in the network [101]. b) Mobility vs. channel length for random network on nanotubes, including the purified nanotubes with different purifications and CVD-grown random network. 99%, 98% semiconducting tube inks and also CVD-grown random network show improvement in the mobility with increasing the channel length. 95% semiconducting nanotube ink shows inverse relation between mobility and channel length. The density of the presented samples are different and also the contact resistance has not been taken into account [13, 24, 68, 72].

In addition, Figure 3.10b summarizes the state of the art of nanotube networks, and includes data from 3 different labs including our lab (my results, also presented above) [13, 24, 68, 72] as well as both CVD grown, and purified SWNT inks. The results indicate that the length dependence is typically observed, is mild, and is not explained by current theories. In summary, for the length dependence of the mobility:

- Experiments consistently observe length dependent mobility

- Phenomenon not understood quantitatively or qualitatively
- No universal trend
- Not purely an alignment effect

3.5.1.2. Scaling with density

The scaling of the critical performance parameters like the mobility and on/off ratio has been studied mostly for CVD grown nanotube networks, which are random with a fraction of metallic nanotubes. The effect of the density on the on/off ratio has been studied fairly carefully by only a few labs (including my work) [13, 26, 93]. Generally speaking, if the density of the metallic nanotubes is below the percolation threshold, but the density of semiconducting nanotubes is above the percolation threshold, then the on/off ratio can be quite large. (Figure 3.11a shows SEM images of different densities.) However, finding and tuning this transition for unpurified materials is very difficult, because the window of parameter space is small. (The metallic density is only 2X lower than the semiconducting density.) That transition was achieved only by two groups in the last year, Maryland [93] and Ohno/Japan [26]. Maryland made a detailed study of the density dependence of CVD grown networks, and found a sharp transition from low to high on/off ratio at a tube density of about 1 tubes/μm^2, and their results are plotted in Figure 3.11b. Ohno's study was less systematic but found the transition at about 10 tubes/μm^2 (using longer CVD grown tubes), although density dependence of the on/off ratio was not reported.

In the case of purified semiconducting nanotube inks, one would expect the metallic nanotube fraction to be 10-100X smaller than the semiconducting fraction, so that it would be well below the percolation threshold at almost all tube densities. The density dependence of the on/off ratio of purified SWNT networks is plotted in Figure 3.11b [13]. (Similar behavior is

observed for DEP aligned purified nanotubes vs. linear density [86].) However, we found that the density dependence of the on/off ratio is less severe, for reasons that are currently not understood. The answer may be related to the average nanotube length, however this issue is important to address with future experiments. At the very least, now it has been quantified allowing a roadmap to applications, if albeit a phenomenological roadmap.

Next, we discuss the effect of tube density on mobility. Although higher tube density will clearly give higher on current, the effect on mobility is not so clear. In fact, classical semiconducting materials sometimes have lower mobility for higher density, in both 2d and 3d systems. Therefore, the effect of density on mobility should be investigated numerically based on simulations, and we are unaware of any general theory on the scaling between mobility and density. Again, in such a situation, in order to drive the technology forward, one most resort to phenomenological characterizations, as performed here. Figure 3.11c demonstrates mobility vs. density. To our knowledge, this is the only such study to date of any nanotube network system. These results clearly indicate a trend of increasing mobility with increasing density. (Again, similar behavior is observed for DEP aligned purified nanotubes vs. linear density [86]). However, as discussed above, this also leads to a decreasing on/off ratio. Therefore, the coupled effects of these two parameters give rise to a competition between mobility and on/off ratio. By tuning the density, the user can adjust the tradeoff between these two parameters. Therefore, the quantitative tradeoff is important to establish, which I will discuss next.

To summarize regarding the density dependence, it is:

- Recently quantified
- Not understood

- Severe impediment to technology, needing further study.

3.5.1.3. On/off ratio vs. mobility

As discussed, by changing the density, the on/off ratio and the mobility both change. Therefore, one can map out (through a careful density dependent study) the on/off ratio as a function of mobility. Unfortunately, there are many variables that also can affect the mobility so that it is difficult to compare one lab's work to another from the literature. For this reason, a systematic study changing only the density changes (keeping all other variables constant) is the best way to establish trends. We have in fact recently performed such a study as shown in this chapter and also in [13]. Our experiments show a clear trend, and also establish some of the highest mobilities for a given density ever reported. This illustrates the potential of purified semiconducting nanotube inks. Surprisingly, when the other limited data from other groups [13, 24, 69-71] is compiled on the same plot, the trend becomes clear when plotted on the same graph (Figure 3.12, blue data points). Although all the presented research works use purified nanotube inks, the purification method and percentage (ratio of metallic to semiconducting), deposition techniques (drop-dry, spin-coating, DEP, etc.) and fabrication steps vary from one to another, which should be considered as well. When compiling similar data [46-48, 90, 100-102] from nanotube inks made of un-purified nanotubes, a similar trend emerges, but with a much lower mobility for a given on/off ratio, as also seen in Figure 3.12 (red data points).

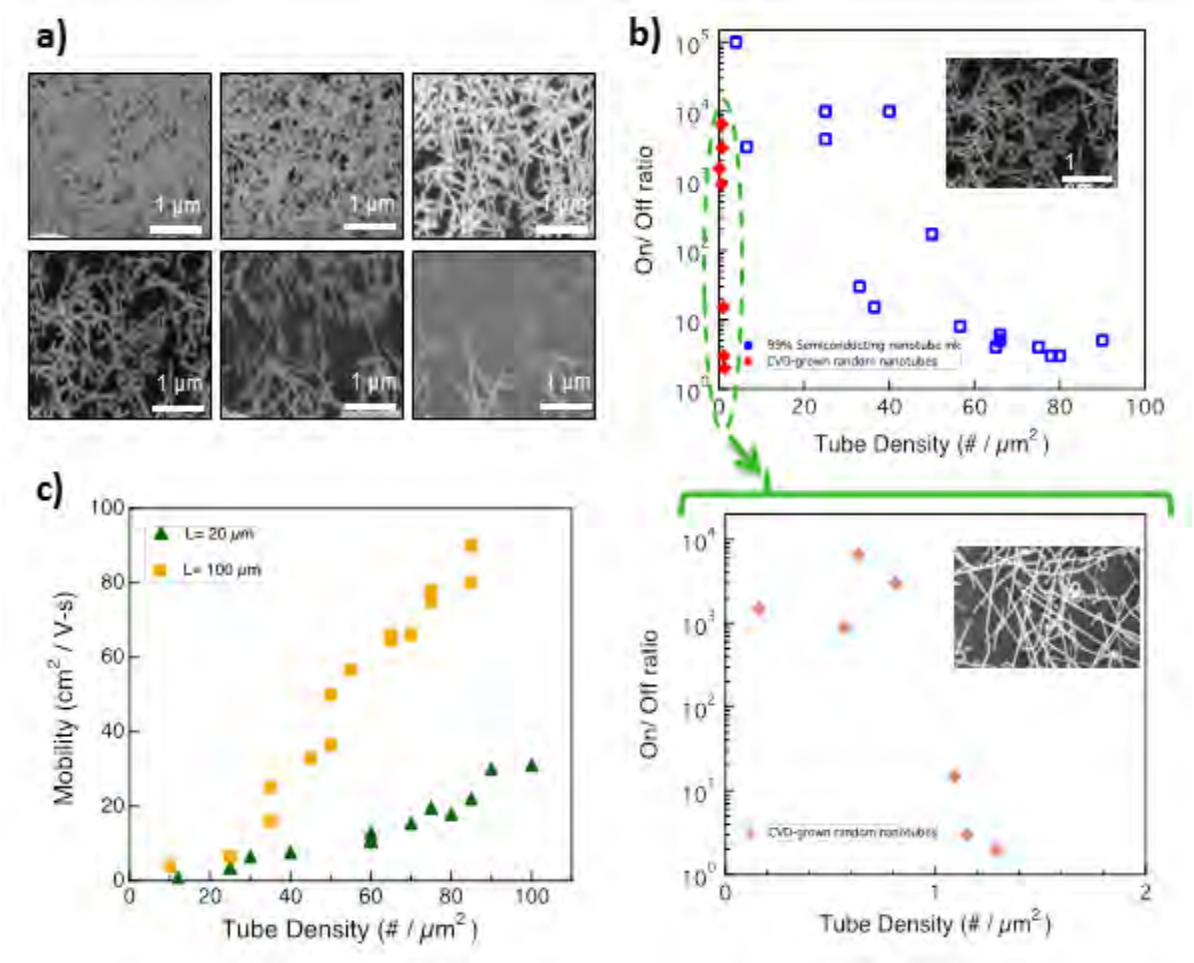

Figure 3.11. Tube density impact [3]. a) SEM images of different tube densities [13]. b) Impact of tube density on the on/off ratio of devices with channel length of 100 µm and channel width of 200 µm for 99% semiconducting nanotube ink [13] and also random network of CVD grown nanotubes [93]. On/off ratio decreases with the increase in nanotube density especially when the percolation threshold is passed. c) Mobility as a function of nanotube density for 99% semiconducting nanotube ink with two different channel lengths of 100 µm and 20 µm with a fixed channel width of 200 µm [13].

The next step is to determine if such a trend exists for CVD grown nanotube networks [26, 66, 68, 92, 93, 106], and the answer is also yes (Figure 3.12, green data points), although the scatter of data is larger, as there are many more reported experiments on this older technology, with many more parameters changing from experiment to experiment, other than just the density. Note that researchers tend to quote the best on/off ratio and best mobility in one sentence, but in

reality they are not achieved simultaneously, so that the literature must be carefully read to compare different techniques. Nonetheless, the trend clearly show a similar trend to the networks deposited from solution, which makes sense, as both result in a random network of 1/3 metallic 2/3 semi nanotubes. A recent advance was achieved by Ohno [26] of mobility at a given on/off ratio for un-purified nanotubes. Although they do not explain the reasons for the improved result in their paper, it is epected that the improvement may be due to the long nanotubes (10 μm), which results in higher mobilities for a given on-off ratio. This is clearly an avenue for improved ink chemistry, to be explored in the future. Thus, Figure 3.12 represents the collective knowledge to date of the relationship between mobility and on/off ratio for nanotube inks, and forms an important roadmap for the future of the field.

As it has been repeatedly emphasized, a clear and comprehensive, predictive theory for the electrical properties of nanotube networks does not exist. However, a trend can clearly be observed looking at the data from hundreds of researchers around the world, that the mobility vs. on/off ratio is significantly improved for purified semiconducting nanotube ink, over and above that of mixtures. Thus, summarizing, the following main points:

- Density seems to be KEY ingredient.
- Dependence not quantitatively predicted by theory.
- Density can be engineered.
- Uniformly shows purified inks improve mobility for a given on/off ratio.
- Phenomenological roadmap for the industry exists, and is subject to continuous improvement.
- May improve with more fundamental materials studies.

3.5.2. PROSPECTS AND CHALLENGES

3.5.2.1. Performance limits can be improved by ink chemistry

At this point, we will speculate about routes and prospects for improved mobility and on/off ratios. It is clear, from studies on dense aligned arrays of CVD grown nanotubes, that at least 10X improvement in mobility is in principle possible, from 100 to 1000 cm^2 / V-s, for nanotube networks. Whether this can be achieved with random arrays is unknown, but not out of the question. Next, the purity of the ink seems to improve the overall mobility for a given on/off ratio, and so we speculate in Figure 3.12 that an improved ink purity will drive the blue curve up, and to the right. How much further the curve can be driven, and how high the mobility can eventually reach, is currently uncertain, and an important topic for further research. A clear possible route to improved mobility is to use longer SWNTs. This has been shown by recent work of both purified [107] and CVD grown [26] networks where longer tubes gave substantially larger mobilities for a given on/off ratio. In [107], for example, a mobility of > 100 cm^2 / V-s at 10^5 on/off ratio was observed after selective gel based removal of short nanotubes, a much higher mobility than other groups that use purified, but short SWNTs (Figure 3.12). Similarly, the mobility of CVD grown tubes was dramatically improved by the same group [26] for a given on/off ratio by using 10 μm long SWNTs, much longer than other researchers typically synthesize.

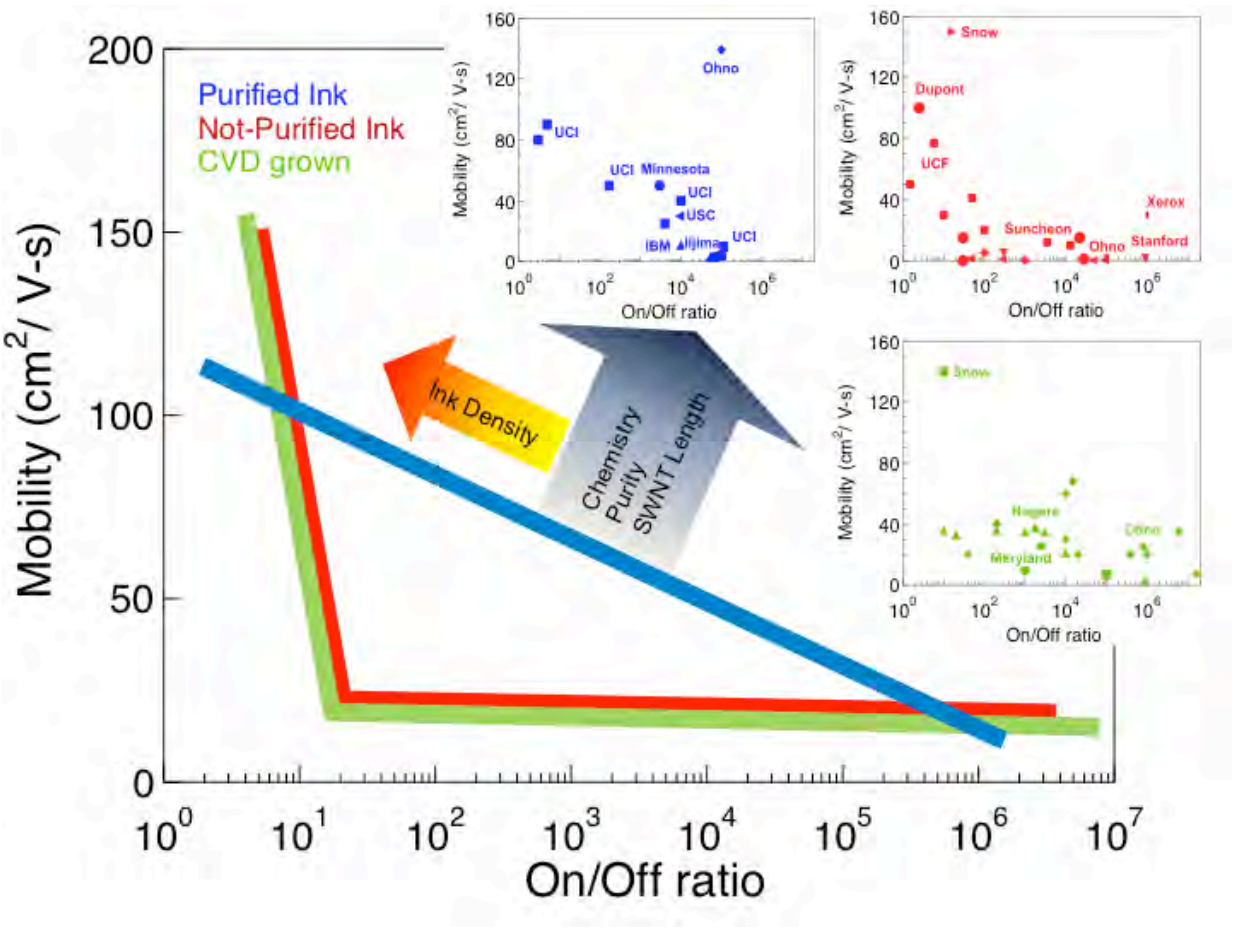

Figure 3.12. Mobility and on/off ratio relationship. The solid lines are limits for different nanotube networks. The green line (CVD-grown) and red line (non-purified inks) show similar trends with a drastic drop on on/off ratio due to presence of metallic tubes. The blue line (purified ink) on the other hand shows smooth and controllable trend between mobility and on/off ratio. As hypothesized in the text, by improving the purity of the nanotube ink it is possible to push the limit to higher mobility for a given on/off ratio. In addition, network density is shown as a controlling factor (for a fixed purity) to change the mobility and on/off ratio. The inset figures show the data points for each different method. Purified ink (blue) [13, 24, 69-71, 107], non-purified ink (red) [40, 45-49, 59, 60], and CVD-grown random network (green) [26, 66, 68, 92, 93, 106]. Note the Florida data series [59, 60] for non-purified ink involves successive breakdown of metallic tubes, so really involves a gradual transition from the red line (unpurified) to the blue line (purified) as the metallic nanotubes are removed by breakdown, although the data points are only plotted in red

A critical component for manufacturing is the ink chemistry. While the studies of deposited nanotube networks have been reviewed and studied in depth, a critical problem in high

throughput manufacturing is the ink viscosity and especially drying time [108]. For roll to roll printing, the drying time should be short enough to allow for high speed printing. Most published studies do not address this issue, but it is critical for industry to address for future printing technologies. A separate issue still to be completely investigated is the role of the substrate on electrical properties. For materials under consideration as flexible substrates (such as PET), to date there has been little evidence of degradation in mobility as compared to SiO_2 on silicon wafers. This is somewhat paradoxical, as the PET has surface roughness typically comparable to or larger than the nanotube diameter, whereas SiO_2 is usually smooth. This needs further study, but at present does not seem to be a major practical impediment to high performance inks. Finally, the effect of the surfactant (and their removal), needed for acqueous solutions, on the electronic properties of the deposited networks needs to be investigated. To date only one such comprehensive study has been attempted (by our group) [75], but more research is needed to completely quantify this critical link between the chemical and electronic properties of nanotubes.

Our vision for this needed emphasis is shown in Figure 3.1. Of all the ingredients and technologies that go into manufacturing nanotube network electronics, those that involve the ink chemistry are the least investigated, and the most fruitful component of the supply chain to attack in terms of return on investment of improved performance and cost.

3.5.2.2. Applications will be decided by cost considerations. Yields must be increased for SWNTs to be competitive.

Organic materials are also used vastly for printed electronic circuits [12, 109, 110]. The advantage of these materials is mechanical flexibility, ease of use and compatibility with low temperature processes and flexible substrates. However the stability of these devices towards air,

moisture, and light exposure needs further effort. In addition, the electrical performance of such devices requires improvement especially in terms of *mobility*. Although the organic field effect transistors show very high on/off ratio (more than 10^7 in some cases) they suffer from very low mobilities in order of ~1 cm^2 / V-s [12, 111] This low carrier mobility makes organic FETs unsuitable for some high current, high-speed printed electronics applications. Apart from process compatibility and electrical performance, cost is a critical issue to be considered in applications. So far, nanotube-based devices cannot compete with organic transistors in cost, but performance is orders of magnitude higher. A detailed economic model that allows the cost performance tradeoff to be analyzed is possible and important for commercial entities and engineering teams looking to apply the technology in the field.

3.5.2.3. High performance RF devices are a low hanging fruit

In previous sections some demonstrations of solution-based nanotube circuits in DC and low frequency (~100 Hz) have been discussed. However, the intrinsic radio frequency characteristic of individual nanotubes has been analyzed, showing capability of exceeding THz frequencies [2, 112]. The full potential of solution-based random network of nanotubes for the applications in high performance RF devices has not yet been demonstrated, although devices made from random networks in the 10 GHz range have already been demonstrated [99, 108, 109]. The main issue for random networks of semiconducting nanotubes is the potential impact of the reduced mobility compared to individual tubes or aligned arrays. The very small channel lengths required to obtain high frequencies (see the frequency and channel length relation in the "theoretical background" section) is a critical milestone for available printing techniques. Although techniques for making printed circuits typically achieve resolutions (and hence gate lengths) of ~10 μm, the recent introduction of self-aligned techniques to the manufacture of printed circuits

has allowed submicrometre gate lengths to be achieved, even in inkjet printed devices [113]. Thus, high performance RF devices are a clear potential application for purified nanotube inks.

3.5.2.4. System technology demonstrations

The first comprehensive system demonstration using carbon nanotube semiconducting inks was presented in 2010, and consisted of roll-to-roll printed RFID tag. This system included a printable antenna, rectifier, and ring oscillator (~ 100 Hz) on plastic foils and operating at 13.56-MHz as a 1-bit RF tag [48]. The highest mobilities of the nanotubes used in that work are ~ 5 cm^2 / V-s, at an on/off ratio of 100; the number of active TFTs is ~ 10. Because it is a roll-to-roll (Gravure) printing process, throughput is high. A higher level of integrated circuit demonstrations with nanotube networks of higher mobility (and hence operation frequency) by about an order of magnitude (80 cm^2 / V-s, and 1 kHz) were demonstrated with very high levels of integration (~ 10,000 TFTs) [66], allowing for demonstration of basic logic circuitry (inverter, NOR, NAND). Although a higher level of integration, several steps require lithography and so the throughput is not purely roll-to-roll. Besides, here they used as-grown SWNT material whereas in roll-to-roll printing process, purified ink was used. Therefore, there is clearly room for improvement in system demonstrations in the future.

Recent work has attempted to fabricate printed circuits using purified nanotube inks, and this has allow for the demonstration of inverters, NAND gates, and ring oscillators on both polyimide and SiO_2 substrates with < 3 V operation [70]. The semiconducting carbon nanotube network and high capacitance ion gel gate dielectric is patterned by ink-jet printing. In their work, they immerse the substrates in a 1 mM ethanol solution of hexadecanethiol (for polyimide substrates) or anthracene thiol (for SiO_2 substrates) for 12 h (which is a long time for large-scale printed

circuits) in order to make a self-assembled monolayer on the Au electrodes. Printing was accomplished in ambient conditions using a commercially available aerosol jet printing system. The water-based SWNT ink was printed on the channel area with a printing speed of 3 mm/s (5 mm/s for low-coverage films). The measurements are also performed in vacuum due to sensitivity of the gel electrolyte (used as dielectric) to moisture. This provides system level demonstration of purified semiconducting inks in circuits. Although several challenges remain, all three of these results indicate the potential of nanotube ink in a variety of circuits and systems.

3.6. CONCLUSION

Nanotube based semiconducting ink has been demonstrated to be technically superior in terms of mobility to any other semiconducting ink. Combined with recent purification technologies to remove metallic nanotubes, the on/off ratio has been addressed with several techniques. Based on several studies, we have attempted to provide the first draft in this chapter of a comprehensive technology roadmap that summarizes my research outcomes as well as state of the art performance that can be expected for different applications. In addition, the field is continuing to develop, and additional advances are announced often, so that this framework should be updated frequently, although the fundamentals laid out in this work remain. Several systems level demonstrations have shown the potential application of semiconducting nanotube ink in circuits of increasing complexity and performance, while simultaneously addressing the issue of manufacturability.

The potential for improved performance and lower cost systems requires additional effort to realize the projected advantages in various applications. We have outlined many of the "choke points" in the supply chain, starting from the fundamental material synthesis and ending with the system properties. We have argued that, while all areas of this chain should be addressed, the ink chemistry and composition is the least explored technologically and the most fruitful avenue to attack to exploit the potential advantages of semiconducting nanotube inks. Once this has been addressed, future work will be required to find the appropriate points of insertion into existing and future systems level applications.

3.7. FUTURE PROPOSALS

Presented work in this chapter shows a promising future for carbon nanotube ink based printed technology. Among the future proposed works that can be done in our lab at UCI are the study of printed devices on plastic substrate and system level fabrication of basic logic circuits (e.g. Nor, Nand, etc.) and monitor the performance of such circuits. Also the high frequency application of these devices can be explored by the means of the e-beam lithography system although this approach is not scalable in printed electronics. Top gate design is another path which is yet unknown but it can be studied on the basis of the primary results established by this presented work.

3.8. ACKNOWLEDGMENT

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3.9. REFERENCES AND NOTES

[1] J. W. G. Wildoer, L. C. Venema, A. G. Rinzler, R. E. Smalley, and C. Dekker, "Electronic structure of atomically resolved carbon nanotubes," *Nature,* vol. 391, pp. 59-62, 1998.

[2] C. Rutherglen, D. Jain, and P. Burke, "Nanotube electronics for radiofrequency applications," *Nature Nanotechnology,* vol. 4, pp. 811-819, 2009.

[3] N. Rouhi, D. Jain, and P. Burke, "High-Performance Semiconducting Nanotube Inks: Progress and Prospects," *ACS Nano,* 2011.

[4] P. Avouris, Z. Chen, and V. Perebeinos, "Carbon-based electronics," *Nature Nanotechnology,* vol. 2, pp. 605-615, 2007.

[5] A. Naeemi and J. D. Meindl, "Carbon Nanotube Interconnects," *Annual Review of Materials Research,* vol. 39, pp. 255-275, 2009.

[6] Z. Wu, Z. Chen, X. Du, J. M. Logan, J. Sippel, M. Nikolou, K. Kamaras, J. R. Reynolds, D. B. Tanner, and A. F. Hebard, "Transparent, conductive carbon nanotube films," *Science,* vol. 305, p. 1273, 2004.

[7] L. Ding, A. Tselev, J. Wang, D. Yuan, H. Chu, T. P. McNicholas, Y. Li, and J. Liu, "Selective Growth of Well-Aligned Semiconducting Single-Walled Carbon Nanotubes," *Nano Letters,* vol. 9, pp. 800-805, 2009.

[8] W. W. Zhou, C. Rutherglen, and P. J. Burke, "Wafer Scale Synthesis of Dense Aligned Arrays of Single-Walled Carbon Nanotubes," *Nano Research,* vol. 1, pp. 158-165, Aug 2008.

[9] M. Hersam, "Progress towards monodisperse single-walled carbon nanotubes," *Nature Nanotechnology,* vol. 3, pp. 387-394, 2008.

[10] J. Liu and M. C. Hersam, "Recent Developments in Carbon Nanotube Sorting and Selective Growth," *MRS Bulletin,* vol. 35, pp. 315-321, Apr 2010.

[11] NanoIntegris, Inc.,. (year, August 6, 2011). Available: http://www.nanointegris.com/en/semiconducting

[12] Z. Bao and J. Locklin, *Organic Field-Effect Transistors*. Boca Raton: CRC Press, 2007.

[13] N. Rouhi, D. Jain, K. Zand, and P. J. Burke, "Fundamental Limits on the Mobility of Nanotube-Based Semiconducting Inks," *Advanced Materials,* vol. 23, pp. 94-99, 2011.

[14] E. S. Snow, P. M. Campbell, M. G. Ancona, and J. P. Novak, "High-mobility carbon-nanotube thin-film transistors on a polymeric substrate," *Applied Physics Letters,* vol. 86, pp. -, Jan 17 2005.

[15] Q. Cao and J. A. Rogers, "Ultrathin Films of Single-Walled Carbon Nanotubes for Electronics and Sensors: A Review of Fundamental and Applied Aspects," *Advanced Materials,* vol. 21, pp. 29-53, Jan 5 2009.

[16] M. D. Lay, J. P. Novak, and E. S. Snow, "Simple route to large-scale ordered arrays of liquid-deposited carbon nanotubes," *Nano Letters,* vol. 4, pp. 603-606, Apr 2004.

[17] L. Hu, D. S. Hecht, and G. Gruner, "Percolation in transparent and conducting carbon nanotube networks," *Nano Letters,* vol. 4, pp. 2513-2517, Dec 2004.

[18] M. A. Meitl, Y. X. Zhou, A. Gaur, S. Jeon, M. L. Usrey, M. S. Strano, and J. A. Rogers, "Solution casting and transfer printing single-walled carbon nanotube films," *Nano Letters,* vol. 4, pp. 1643-1647, Sep 2004.

[19] S. J. Oh, Y. Cheng, J. Zhang, H. Shimoda, and O. Zhou, "Room-temperature fabrication of high-resolution carbon nanotube field-emission cathodes by self-assembly," *Applied Physics Letters,* vol. 82, pp. 2521-2523, Apr 14 2003.

[20] J. U. Park, M. A. Meitl, S. H. Hur, M. L. Usrey, M. S. Strano, P. J. A. Kenis, and J. A. Rogers, "In situ deposition and patterning of single-walled carbon nanotubes by Laminar flow and controlled flocculation in microfluidic channels," *Angewandte Chemie-International Edition,* vol. 45, pp. 581-585, 2006.
[21] X. L. Li, L. Zhang, X. R. Wang, I. Shimoyama, X. M. Sun, W. S. Seo, and H. J. Dai, "Langmuir-Blodgett assembly of densely aligned single-walled carbon nanotubes from bulk materials," *Journal of the American Chemical Society,* vol. 129, pp. 4890-+, Apr 25 2007.
[22] Q. Cao, S. H. Hur, Z. T. Zhu, Y. G. Sun, C. J. Wang, M. A. Meitl, M. Shim, and J. A. Rogers, "Highly bendable, transparent thin-film transistors that use carbon-nanotube-based conductors and semiconductors with elastomeric dielectrics," *Advanced Materials,* vol. 18, pp. 304-309, Feb 3 2006.
[23] N. Rouhi, Jain, D., Zand, K. & Burke, P. J., "All-semiconducting nanotube devices for RF and microwave applications," in *Proceedings of IEEE IMS*, Anaheim, 2010, pp. 1420-1422.
[24] C. Wang, J. L. Zhang, K. M. Ryu, A. Badmaev, L. G. De Arco, and C. W. Zhou, "Wafer-Scale Fabrication of Separated Carbon Nanotube Thin-Film Transistors for Display Applications," *Nano Letters,* vol. 9, pp. 4285-4291, Dec 2009.
[25] M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, and M. C. Hersam, "Sorting carbon nanotubes by electronic structure using density differentiation," *Nature Nanotechnology,* vol. 1, pp. 60-65, Oct 2006.
[26] D. Sun, M. Y. Timmermans, Y. Tian, A. G. Nasibulin, E. I. Kauppinen, S. Kishimoto, T. Mizutani, and Y. Ohno, "Flexible high-performance carbon nanotube integrated circuits," *Nature Nanotechnology,* vol. 6, pp. 156-161, February 2011.
[27] Y. Li, W. Kim, Y. Zhang, M. Rolandi, D. Wang, and H. Dai, "Growth of single-walled carbon nanotubes from discrete catalytic nanoparticles of various sizes," *Journal of Physical Chemistry B,* vol. 105, pp. 11424-11431, 2001.
[28] C. L. Cheung, A. Kurtz, H. Park, and C. M. Lieber, "Diameter-controlled synthesis of carbon nanotubes," *Journal of Physical Chemistry B,* vol. 106, pp. 2429-2433, 2002.
[29] D. Ciuparu, Y. Chen, S. Lim, G. L. Haller, and L. Pfefferle, "Uniform-diameter single-walled carbon nanotubes catalytically grown in cobalt-incorporated MCM-41," *Journal of Physical Chemistry B,* vol. 108, pp. 503-507, Jan 15 2004.
[30] Y. Chen, D. Ciuparu, S. Y. Lim, Y. H. Yang, G. L. Haller, and L. Pfefferle, "Synthesis of uniform diameter single-wall carbon nanotubes in Co-MCM-41: effects of the catalyst prereduction and nanotube growth temperatures," *Journal of Catalysis,* vol. 225, pp. 453-465, Jul 25 2004.
[31] S. M. Bachilo, L. Balzano, J. E. Herrera, F. Pompeo, D. E. Resasco, and R. B. Weisman, "Narrow (n,m)-Distribution of Single-Walled Carbon Nanotubes Grown Using a Solid Supported Catalyst," *Journal of the American Chemical Society,* vol. 125, pp. 11186-11187, 2003.
[32] G. Lolli, L. Zhang, L. Balzano, N. Sakulchaicharoen, Y. Tan, and D. Resasco, "Tailoring (n,m) Structure of Single-Walled Carbon Nanotubes by Modifying Reaction Conditions and the Nature of the Support of CoMo Catalysts," *Journal of Physical Chemistry B,* vol. 110, pp. 2108-2115, 2006.
[33] B. Wang, C. H. P. Poa, L. Wei, L. J. Li, Y. H. Yang, and Y. Chen, "(n,m) selectivity of single-walled carbon nanotubes by different carbon precursors on co-mo catalysts," *Journal of the American Chemical Society,* vol. 129, pp. 9014-9019, Jul 25 2007.
[34] W. Kim, A. Javey, R. Tu, J. Cao, Q. Wang, and H. Dai, "Electrical contacts to carbon nanotubes down to 1 nm in diameter," *Applied Physics Letters,* vol. 87, pp. 173101-1-3, 2005.
[35] Z. Chen, J. Appenzeller, J. Knoch, Y.-M. Lin, and P. Avouris, "The Role of Metal-Nanotube Contact in the Performance of Carbon Nanotube Field-Effect Transistors," *Nano Letters,* vol. 5, pp. 1497-1502, 2005.
[36] D. S. Goodsell, *Bionanotechnology : lessons from nature*. Hoboken: Wiley-Liss, 2004.
[37] S. N. Kim, Z. Kuang, J. G. Grote, B. L. Farmer, and R. R. Naik, "Enrichment of (6, 5) single wall carbon nanotubes using genomic DNA," *Nano Letters,* vol. 8, pp. 4415-4420, 2008.
[38] M. C. Hersam, "Materials science: Nanotubes sorted using DNA," *Nature,* vol. 460, pp. 186-187, 2009.
[39] X. M. Tu, S. Manohar, A. Jagota, and M. Zheng, "DNA sequence motifs for structure-specific recognition and separation of carbon nanotubes," *Nature,* vol. 460, pp. 250-253, Jul 9 2009.
[40] Y. Asada, Y. Miyata, K. Shiozawa, Y. Ohno, R. Kitaura, T. Mizutani, and H. Shinohara, "Thin-Film Transistors with Length-Sorted DNA-Wrapped Single-Wall Carbon Nanotubes," *Journal of Physical Chemistry C,* vol. 115, pp. 270-273, 2010.
[41] L. Zheng, D. Jain, and P. Burke, "Nanotube Peptide Interactions on a Silicon Chip," *Journal of Physical Chemistry C,* vol. 113, pp. 3978-3985, 2009.

[42] H. Xie, E. J. Becraft, R. H. Baughman, A. B. Dalton, and G. R. Dieckmann, "Ranking the affinity of aromatic residues for carbon nanotubes by using designed surfactant peptides," *Journal of Peptide Science,* vol. 14, pp. 139-151, 2008.

[43] G. Grigoryan, Y. H. Kim, R. Acharya, K. Axelrod, R. M. Jain, L. Willis, M. Drndic, J. M. Kikkawa, and W. F. DeGrado, "Computational Design of Virus-Like Protein Assemblies on Carbon Nanotube Surfaces," *Science,* vol. 332, pp. 1071-1076, May 27, 2011 2011.

[44] M. Lay, J. Novak, and E. Snow, "Simple Route to Large-Scale Ordered Arrays of Liquid-Deposited Carbon Nanotubes," *Nano Letters,* vol. 4, pp. 603-606, 2004.

[45] E. S. Snow, P. M. Campbell, M. G. Ancona, and J. P. Novak, "High-mobility carbon-nanotube thin-film transistors on a polymeric substrate," *Applied Physics Letters,* vol. 86, p. 033105, Jan 17 2005.

[46] M. Kanungo, H. Lu, G. G. Malliaras, and G. B. Blanchet, "Suppression of Metallic Conductivity of Single-Walled Carbon Nanotubes by Cycloaddition Reactions," *Science,* vol. 323, pp. 234-237, Jan 9 2009.

[47] M. Kanungo, G. G. Malliaras, and G. B. Blanchet, "High performance organic transistors: Percolating arrays of nanotubes functionalized with an electron deficient olefin," *Applied Physics Letters,* vol. 97, pp. 053304-1-3, Aug 2 2010.

[48] M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, J. M. Tour, and G. Cho, "All-Printed and Roll-to-Roll-Printable 13.56-MHz-Operated 1-bit RF Tag on Plastic Foils," *IEEE Transactions on Electron Devices,* vol. 57, pp. 571-580, Mar 2010.

[49] M. C. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim, and Z. Bao, "Self-Sorted, Aligned Nanotube Networks for Thin-Film Transistors," *Science,* vol. 321, pp. 101-104, July 4, 2008 2008.

[50] M. Shiraishi, T. Takenobu, T. Iwai, Y. Iwasa, H. Kataura, and M. Ata, "Single-walled carbon nanotube aggregates for solution-processed field effect transistors," *Chemical Physics Letters,* vol. 394, pp. 110-113, Aug 11 2004.

[51] K. Bradley, J. C. P. Gabriel, and G. Grüner, "Flexible nanotube electronics," *Nano Letters,* vol. 3, pp. 1353-1355, 2003.

[52] S. Auvray, V. Derycke, M. Goffman, A. Filoramo, O. Jost, and J. P. Bourgoin, "Chemical optimization of self-assembled carbon nanotube transistors," *Nano Letters,* vol. 5, pp. 451-455, Mar 2005.

[53] J. Liu, M. J. Casavant, M. Cox, D. A. Walters, P. Boul, W. Lu, A. J. Rimberg, K. A. Smith, D. T. Colbert, and R. E. Smalley, "Controlled deposition of individual single-walled carbon nanotubes on chemically functionalized templates," *Chemical Physics Letters,* vol. 303, pp. 125-129, Apr 2 1999.

[54] D. Chattopadhyay, L. Galeska, and F. Papadimitrakopoulos, "A route for bulk separation of semiconducting from metallic single-wall carbon nanotubes," *Journal of the American Chemical Society,* vol. 125, pp. 3370-3375, Mar 19 2003.

[55] M. Vosgueritchian, M. C. LeMieux, D. Dodge, and Z. Bao, "Effect of Surface Chemistry on Electronic Properties of Carbon Nanotube Network Thin Film Transistors," *Acs Nano,* vol. 4, pp. 6137-6145, 2011.

[56] P. C. Collins, M. S. Arnold, and P. Avouris, "Engineering carbon nanotubes and nanotube circuits using electrical breakdown," *Science,* vol. 292, pp. 706-709, Apr 27 2001.

[57] H. Wei, N. Patil, J. Zhang, A. Lin, H.-Y. Chen, H.-S. Philip Wong, and S. Mitra, "Efficient Metallic Carbon Nanotube Removal Readily Scalable to Wafer-Level VLSI CNFET Circuits," in *VLSI Technology Digest*, 2010, pp. 237-238.

[58] I. Amlani, N. Pimparkar, K. Nordquist, D. Lim, S. Clavijo, Q. Zhengfang, and R. Emrick, "Automated Removal of Metallic Carbon Nanotubes in a Nanotube Ensemble by Electrical Breakdown," in *Nanotechnology, 2008. NANO '08. 8th IEEE Conference on*, 2008, pp. 239-242.

[59] P. Stokes, E. Silbar, Y. M. Zayas, and S. I. Khondaker, "Solution processed large area field effect transistors from dielectrophoreticly aligned arrays of carbon nanotubes," *Applied Physics Letters,* vol. 94, p. 113104, 2009.

[60] S. Shekhar, P. Stokes, and S. I. Khondaker, "Ultrahigh Density Alignment of Carbon Nanotube Arrays by Dielectrophoresis," *Acs Nano,* vol. 5, pp. 1739–1746, 2011.

[61] S. Shekhar, M. Erementchouk, M. N. Leuenberger, and S. I. Khondaker, "Correlated electrical breakdown in arrays of high density aligned carbon nanotubes," *Applied Physics Letters,* vol. 98, p. 243121, 2011.

[62] M. S. Strano, C. A. Dyke, M. L. Usrey, P. W. Barone, M. J. Allen, H. W. Shan, C. Kittrell, R. H. Hauge, J. M. Tour, and R. E. Smalley, "Electronic structure control of single-walled carbon nanotube functionalization," *Science,* vol. 301, pp. 1519-1522, Sep 12 2003.

[63] L. An, Q. A. Fu, C. G. Lu, and J. Liu, "A simple chemical route to selectively eliminate metallic carbon nanotubes in nanotube network devices," *Journal of the American Chemical Society,* vol. 126, pp. 10520-10521, Sep 1 2004.

[64] N. Nair, W. J. Kim, M. L. Usrey, and M. S. Strano, "A structure-reactivity relationship for single walled carbon nanotubes reacting with 4-hydroxybenzene diazonium salt," *Journal of the American Chemical Society,* vol. 129, pp. 3946-3954, Apr 4 2007.

[65] C. M. Yang, K. H. An, J. S. Park, K. A. Park, S. C. Lim, S. H. Cho, Y. S. Lee, W. Park, C. Y. Park, and Y. H. Lee, "Preferential etching of metallic single-walled carbon nanotubes with small diameter by fluorine gas," *Physical Review B,* vol. 73, p. 075419, Feb 2006.

[66] Q. Cao, H. Kim, N. Pimparkar, J. Kulkarni, C. Wang, M. Shim, K. Roy, M. Alam, and J. Rogers, "Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates," *Nature,* vol. 454, pp. 495-500, 2008.

[67] N. Pimparkar, Q. Cao, J. A. Rogers, and M. A. Alam, "Theory and practice of "striping" for improved on/off ratio in carbon nanonet thin film transistors," *Nano Research,* vol. 2, pp. 167-175, 2009.

[68] S. Hur, C. Kocabas, A. Gaur, O. Park, M. Shim, and J. Rogers, "Printed thin-film transistors and complementary logic gates that use polymer-coated single-walled carbon nanotube networks," *Journal of Applied Physics,* vol. 98, pp. 114302-1-6, 2005.

[69] M. Engel, J. P. Small, M. Steiner, M. Freitag, A. A. Green, M. C. Hersam, and P. Avouris, "Thin Film Nanotube Transistors Based on Self-Assembled, Aligned, Semiconducting Carbon Nanotube Arrays," *Acs Nano,* vol. 2, pp. 2445-2452, 2008.

[70] M. Ha, Y. Xia, A. A. Green, W. Zhang, M. J. Renn, C. H. Kim, M. C. Hersam, and C. D. Frisbie, "Printed, Sub 3V Digital Circuits on Plastic from Acqueous Carbon Nanotube Inks," *Acs Nano,* vol. 4, pp. 4388–4395, 2010.

[71] N. Izard, S. Kazaoui, K. Hata, T. Okazaki, T. Saito, S. Iijima, and N. Minami, "Semiconductor-enriched single wall carbon nanotube networks applied to field effect transistors," *Applied Physics Letters,* vol. 92, pp. 243112-1-3, 2008.

[72] C. Wang, J. Zhang, and C. Zhou, "Macroelectronic Integrated Circuits Using High-Performance Separated Carbon Nanotube Thin-Film Transistors," *Acs Nano,* vol. 4, pp. 7123–7132, 2010.

[73] J. Zhang, C. Wang, Y. Fu, Y. Che, and C. Zhou, "Air-Stable Conversion of Separated Carbon Nanotube Thin-Film Transistors from p-Type to n-Type Using Atomic Layer Deposition of High- Oxide and Its Application in CMOS Logic Circuits," *Acs Nano,* vol. 5, pp. 3284–3292, 2011.

[74] N. Pimparkar, C. Kocabas, S. J. Kang, J. Rogers, and M. A. Alam, "Limits of performance gain of aligned CNT over randomized network: Theoretical predictions and experimental validation," *IEEE Electron Device Letters,* vol. 28, pp. 593-595, Jul 2007.

[75] D. Jain, N. Rouhi, C. Rutherglen, C. G. Densmore, S. K. Doorn, and P. J. Burke, "Effect of Source, Surfactant, and Deposition Process on Electronic Properties of Nanotube Arrays," *Journal of Nanomaterials,* pp. 1-7, January 2011.

[76] C. Rutherglen, D. Jain, and P. Burke, "RF resistance and inductance of massively parallel single walled carbon nanotubes: Direct, broadband measurements and near perfect 50 ohm impedance matching," *Applied Physics Letters,* vol. 93, p. 083119, 2008.

[77] X. Li, L. Zhang, X. Wang, I. Shimoyama, X. Sun, W.-S. Seo, and H. Dai, "Langmuir-Blodgett Assembly of Densely Aligned Single-Walled Carbon Nanotubes from Bulk Materials," *Journal of the American Chemical Society,* vol. 129, pp. 4890-4891, 2007.

[78] R. D. Deegan, O. Bakajin, T. F. Dupont, G. Huber, S. R. Nagel, and T. A. Witten, "Capillary flow as the cause of ring stains from dried liquid drops," *Nature,* vol. 389, pp. 827-829, Oct 23 1997.

[79] B. J. Fischer, "Particle convection in an evaporating colloidal droplet," *Langmuir,* vol. 18, pp. 60-67, Jan 8 2002.

[80] Y. O. Popov, "Evaporative deposition patterns: Spatial dimensions of the deposit," *Physical Review E,* vol. 71, p. 036313, Mar 2005.

[81] L. Shmuylovich, A. Q. Shen, and H. A. Stone, "Surface morphology of drying latex films: Multiple ring formation," *Langmuir,* vol. 18, pp. 3441-3445, Apr 30 2002.

[82] R. Krupke, F. Hennrich, H. von Lohneysen, and M. M. Kappes, "Separation of metallic from semiconducting single-walled carbon nanotubes," *Science,* vol. 301, pp. 344-347, Jul 18 2003.

[83] R. Krupke, S. Linden, M. Rapp, and F. Hennrich, "Thin films of metallic carbon nanotubes prepared by dielectrophoresis," *Advanced Materials,* vol. 18, pp. 1468-1468, 2006.

[84] Y. Kim, S. Hong, S. Jung, M. S. Strano, J. Choi, and S. Baik, "Dielectrophoresis of surface conductance modulated single-walled carbon nanotubes using catanionic surfactants," *Journal of Physical Chemistry B,* vol. 110, pp. 1541-1545, Feb 2 2006.

[85] A. L. Louarn, F. Kapche, J.-M. Bethoux, H. Happy, G. Dambrine, V. Derycke, P. Chenevier, N. Izard, M. F. Goffman, and J.-P. Bourgoin, "Intrinsic current gain cutoff frequency of 30 GHz with carbon nanotube transistors," *Applied Physics Letters,* vol. 90, p. 233108, 2007 2007.

[86] B. K. Sarker, S. Shekhar, and S. I. Khondaker, "Semiconducting Enriched Carbon Nanotube Aligned Arrays of Tunable Density and Their Electrical Transport Properties," *Acs Nano,* pp. published on the web July 13, 2011; DOI:10.1021/nn201314t, 2011.

[87] S. Kumar, J. Y. Murthy, and M. A. Alam, "Percolating conduction in finite nanotube networks," *Physical Review Letters,* vol. 95, pp. 066802-1-4, Aug 5 2005.

[88] N. Pimparkar, Q. Cao, S. Kumar, J. Murthy, J. Rogers, and M. Alam, "Current–Voltage Characteristics of Long-Channel Nanobundle Thin-Film Transistors: A "Bottom-Up" Perspective," *IEEE Electron Device Letters,* vol. 28, pp. 157-160, 2007.

[89] N. Pimparkar, J. Guo, and M. A. Alam, "Performance assessment of subpercolating nanobundle network thin-film transistors by an analytical model," *IEEE Transactions on Electron Devices,* vol. 54, pp. 637-644, Apr 2007.

[90] C. Kocabas, N. Pimparkar, O. Yesilyurt, S. J. Kang, M. A. Alam, and J. A. Rogers, "Experimental and theoretical studies of transport through large scale, partially aligned arrays of single-walled carbon nanotubes in thin film type transistors," *Nano Letters,* vol. 7, pp. 1195-1202, May 2007.

[91] N. Pimparkar and M. A. Alam, "A "Bottom-Up" Redefinition for Mobility and the Effect of Poor Tube–Tube Contact on the Performance of CNT Nanonet Thin-Film Transistors," *IEEE Electron Device Letters,* vol. 29, pp. 1037-1039, 2008.

[92] E. S. Snow, J. P. Novak, P. M. Campbell, and D. Park, "Random networks of carbon nanotubes as an electronic material," *Applied Physics Letters,* vol. 82, pp. 2145-2147, Mar 31 2003.

[93] V. Sangwan, A. Behnam, V. Ballarotto, M. Fuhrer, A. Ural, and E. Williams, "Optimizing transistor performance of percolating carbon nanotube networks," *Applied Physics Letters,* vol. 97, pp. 043111-1-3, 2010.

[94] Q. Cao, M. Xia, C. Kocabas, M. Shim, J. Rogers, and S. Rotkin, "Gate capacitance coupling of singled-walled carbon nanotube thin-film transistors," *Applied Physics Letters,* vol. 90, pp. 023516-1-3, 2007.

[95] X. J. Zhou, J. Y. Park, S. M. Huang, J. Liu, and P. L. McEuen, "Band structure, phonon scattering, and the performance limit of single-walled carbon nanotube transistors," *Physical Review Letters,* vol. 95, pp. 146805-1-4, Sep 30 2005.

[96] P. Stokes and S. I. Khondaker, "High quality solution processed carbon nanotube transistors assembled by dielectrophoresis," *Applied Physics Letters,* vol. 96, pp. 083110-1-3, 2010.

[97] Q. Cao and J. Rogers, "Ultrathin Films of Single-Walled Carbon Nanotubes for Electronics and Sensors: A Review of Fundamental and Applied Aspects," *Advanced Materials,* vol. 21, pp. 29-53, 2009.

[98] N. Rouhi, D. Jain, and P. J. Burke, "Nanoscale Devices for Large-Scale Applications," *Ieee Microwave Magazine,* vol. 11, pp. 72-80, Dec 2010.

[99] L. Nougaret, H. Happy, G. Dambrine, V. Derycke, J. P. Bourgoin, A. A. Green, and M. C. Hersam, "80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes," *Applied Physics Letters,* vol. 94, pp. 243505-1-3, 2009.

[100] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H. Y. Chiu, A. Grill, and P. Avouris, "100 GHz Transistors from Wafer-Scale Epitaxial Graphene," *Science,* vol. 327, p. 662, February 5, 2010 2010.

[101] S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," *Nature Nanotechnology,* vol. 2, pp. 230-236, Apr 2007.

[102] M. Eron, S. Lin, D. Wang, M. Schroter, and P. Kempf, "L-band carbon nanotube transistor amplifier," *Electronics Letters,* vol. 47, pp. 265-266, 2011.

[103] C. Wang, A. Badmaev, A. Jooyaie, M. Bao, K. L. Wang, K. Galatsis, and C. Zhou, "Radio Frequency and Linearity Performance of Transistors Using High-Purity Semiconducting Carbon Nanotubes," *Acs Nano,* vol. 5, pp. 4169-4176, 2011.

[104] C. Kocabas, S. Dunham, Q. Cao, K. Cimino, X. Ho, H.-S. Kim, D. Dawson, J. Payne, M. Stuenkel, H. Zhang, T. Banks, M. Feng, S. V. Rotkin, and J. A. Rogers, "High-Frequency Performance of Submicrometer Transistors That Use Aligned Arrays of Single-Walled Carbon Nanotubes," *Nano Letters,* vol. 8, pp. 1937-1943, 2009.

[105] L. Y. Yan, Y. F. Poon, M. B. Chan-Park, Y. Chen, and Q. Zhang, "Individually dispersing single-walled carbon nanotubes with novel neutral pH water-soluble chitosan derivatives," *Journal of Physical Chemistry C,* vol. 112, pp. 7579-7587, May 22 2008.

[106] Q. Cao, M. G. Xia, M. Shim, and J. A. Rogers, "Bilayer organic-inorganic gate dielectrics for high-performance, low-voltage, single-walled carbon nanotube thin-film transistors, complementary logic gates, and p-n diodes on plastic substrates," *Advanced Functional Materials,* vol. 16, pp. 2355-2362, Dec 4 2006.
[107] Y. Miyata, K. Shiozawa, Y. Asada, Y. Ohno, R. Kitaura, T. Mizutani, and H. Shinohara, "Length-sorted semiconducting carbon nanotubes for high-mobility thin film transistors," *Nano Research,* vol. published on the web May 18, 2011; DOI 10.1007/s12274-011-0152-7, pp. 1-8, 2011.
[108] J. Li, T. Unander, A. L. Cabezas, B. Shao, Z. Liu, Y. Feng, E. B. Forsberg, Z. B. Zhang, I. Jõgi, and X. Gao, "Ink-jet printed thin-film transistors with carbon nanotube channels shaped in long strips," *Journal of Applied Physics,* vol. 109, p. 084915, 2011.
[109] M. Singh, H. M. Haverinen, P. Dhagat, and G. E. Jabbour, "Inkjet Printing-Process and Its Applications," *Advanced Materials,* vol. 22, pp. 673-685, Feb 9 2010.
[110] Y. G. Wen and Y. Q. Liu, "Recent Progress in n-Channel Organic Thin-Film Transistors," *Advanced Materials,* vol. 22, pp. 1331-1345, Mar 26 2010.
[111] D. Braga and G. Horowitz, "High-Performance Organic Field-Effect Transistors," *Advanced Materials,* vol. 21, pp. 1473-1486, Apr 20 2009.
[112] P. J. Burke, "AC performance of nanoelectronics: towards a ballistic THz nanotube transistor," *Solid State Electronics,* vol. 40, pp. 1981-1986, 2004 2004.
[113] Y. Y. Noh, N. Zhao, M. Caironi, and H. Sirringhaus, "Downscaling of self-aligned, all-printed polymer thin-film transistors," *Nature Nanotechnology,* vol. 2, pp. 784-789, Dec 2007.

CHAPTER FOUR

GRAPHENE MEMBRANE FABRICATION

4.1. INTRODUCTION

Graphene is known as the thinnest available 2d film in the nature, so far. It is basically a sheet of one-atom layer of carbon. For many years scientists thought that it is not possible or better to say it won't be stable to have a one-atom-thick of any element until 2004 that it was proven experimentally that a one-atom thick layer of carbon exists and can be produced [1, 2]. Graphene is a zero-bandgap material which gives it very unique electrical properties [3-5]. In addition, owing to its excellent mechanical behavior (Young's modulus ~1 TPa [6]) it is highly considered in mechanical resonators [7] and NEMS (nanoelectro-mechanical systems) applications [8]. Besides, it has been proven that because of the one-atom thickness and mechanical stability, graphene can act as one of the best chemical and biological sensing materials especially because it can somehow mimic the cell membrane. In addition, because of its electronic characteristics, it can be used as a zero-bandgap material both for nanoelectronic transistors and nano-size interconnects.

There are several methods to synthesize graphene, among them mechanical exfoliation [1] and CVD (chemical vapor deosition) growth are the most common ones. CVD growth can be done on Ni (resulting mostly multi-layer) [9] or Cu (mainly single-layer films) [10, 11]. Other techniques involve epitaxial growth of graphene over SiC (silicon-carbide) substrate [12, 13] or unzipping/etching nanotubes to get graphene nanoribbons [14, 15]. Some other processes such as hydrazine reduction of graphene oxide paper [16], or sonication in solvents [17], etc. are also proposed in the past few years. However, these methods are either not scalable or don't give a good control over the number of grown layers.

In the mechanical exfoliation technique, usually flakes of graphene/graphite are peeled off of a graphite substrate (HOPG graphite) using scotch tape. Then the tape is placed and rubbed gently on the surface of the target substrate and graphene sheets with different number of layers will be deposited on the substrate. It is known that graphene obtained by this method is so far the best quality available in research scale. Nonetheless, the drawback of this technique in the lack of control over the location and number of layers transferred. Besides, the size of the graphene film is not big enough for large-scale application and cannot be controlled either. The most common technique to study the quality and number of layer in graphene film is taking Raman spectrum of the sample.

In this chapter we will present the methods studied to fabricate single-layer graphene (SLG) and multi-layer graphene (MLG) films. Next, we investigate the options to suspend graphene sheets as big as possible. Graphene is known to have a very high intrinsic mobility of around 200000 cm^2/V-s [18, 19] but in practice the highest mobilities obtained are around 10000 cm^2/V-s [2]. The reason for a drastic degradation in mobility is the scattering phenomena due to the thin size of graphene. One of the most important scattering sources is the substrate on which graphene stands. Therefore there has been a tremendous effort on making suspended graphene and studying the characteristics of such suspended film.

Another idea is to mimic the cell membrane by graphene and put the graphene membrane sensor in an electrolyte to study the sensing capability of graphene membrane as a function of different ions and electrolyte concentrations which in fact requires the fabrication of suspended graphene film at the first place.

4.2. DEVICE FABRICATION

4.2.1. GRAPHENE SYNTHESIZE

At the beginning of this project, the scotch-tape (mechanical exfoliation) method was used to deposit the graphene on the substrate. The results (as shown in Figure 4.1) were graphene flakes with different sizes and different number of layers.

To be able to visually observe graphene flakes under the optical microscope, it was known at the time, that the best substrate is silicon wafer with 300 nm or 90 nm oxide cap (discussed in detail in [20]). Here we used 300 nm thermal oxide on wafer. Other oxide thicknesses need certain filter on the optical microscope to make graphene sheets visible [20]. For the transfer purpose we used HOPG graphite substrate and by the means of scotch tape we peeled of a layer of graphite. Then we put the tape/graphite on the substrate and horizontally rubbed it gently with small vertical pressure using a pen or similar thing.

Next we tried graphene growth using CVD method. It has been shown that large-area single layer graphene is grown on top of thin Copper foil [10]. This method will result in large-are single layer graphene covering the foil with some spots also covered by bilayer and tri-layer graphene films. For this purpose, a 40 μm thick Cu foil was put in the CVD chamber. Chamber is heated up to 900 ^{o}C with a rate of 100 ^{o}C per minute under Ar gas flow (150 sccm). In the next phase we input H_2 gas (5-20 sccm) as well and change the rate to 10 ^{o}C/min to heat up the chamber from 900 to 1000 ^{o}C. Cu foil is left in this temperature for 10 minutes. Afterwards, methane (CH_4) was input the chamber (5-20 sccm) as the base gas to grow graphene for 10-20 minutes. Then the heater is turned off and the sample is cooled down inside the chamber (30-60

minutes). The cooling process is also known as an important factor in the quality of final graphene sheets.

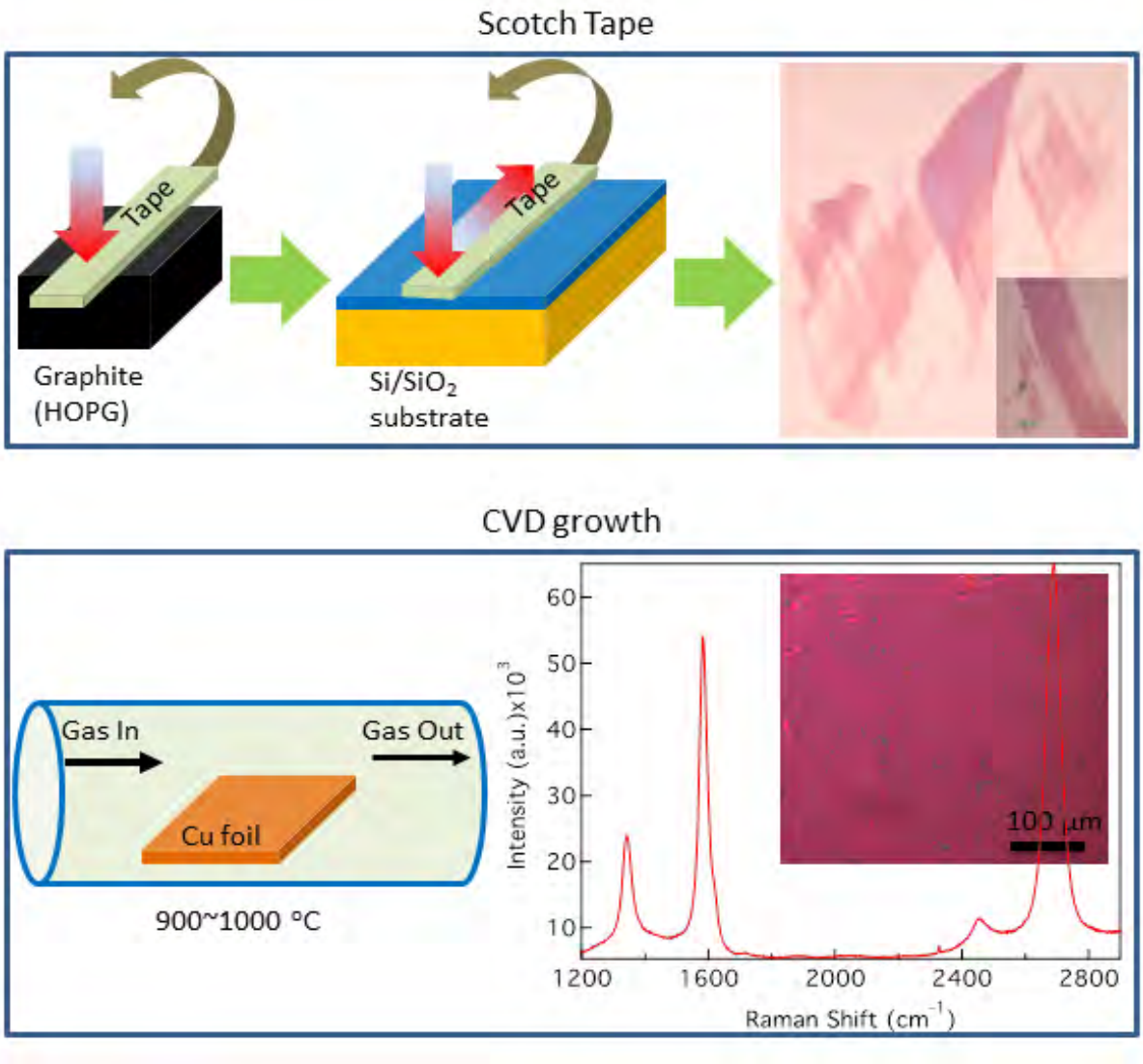

Figure 4.1. Graphene synthesize methods used in my project. Raman spectrum is shown for single layer graphene obtained in our lab.

While we tried CVD in atmospheric pressure, other research works show that low-pressure CVD (LPCVD) will result in better quality graphene (our CVD chamber is now under construction to be converted to LPCVD). To expedite the main objective of this part of project,

which is fabricating suspended graphene membrane, we decided to buy graphene from commercial supplier (graphene supermarket). They provide us with 2"x2" (or 4"x2") Cu foils with graphene grown on top using CVD method. Following the graphene synthesize, we tried transferring it to preferred substrate, but before that the substrate should be prepared and processed.

4.2.2. RAMAN SPECTROSCOPY ANALYSIS

Raman spectroscopy, using 532 nm (wavelength) laser, of the samples demonstrate D, G, and 2D bands' peak of graphene films. D peak is obtained at around 1350 cm^{-1} corresponding to defects while G and 2D peaks location slightly changes with the change in the number of layers. G peak represents the first-order Raman scattering at the Brillouin zone center of graphene however, 2D peak stands for second-order Raman scattering by in-plane optical phonons around the Brillouin zone boundary of graphene film. The average G peak was observed at 1582 cm^{-1} and 2D peak was around 2685 cm^{-1}.

4.2.2.1. Multi-Layer Graphene

To count the number of layers we extracted the ratio of I(G) to I(2D) from Raman spectrum. Based on the recent analysis for mechanically exfoliated graphene as well as graphene grown on Ni [9, 21-24] we estimate the number of layers to be in the range of 3 to 7 layers for our graphene films grown on Ni. However, for n>6 it is hard to count the exact number of layers. To precisely acquire the G/2D peaks intensity ratio, more than 20 spots (in 1x1 cm area) were analyzed to obtain Raman spectrum. The average I(G)/I(2D) is found to be around 1.4 which represents n=4 layers.

4.2.2.2. Single-Layer Graphene

Unlike multilayer graphene, in single layer graphene films the 2D peak (~2690 nm) is sharp and more intense comparing to the G peak (~1590 nm). Similar to multilayer analysis, here in single layer graphene also I(G)/I(2D) peak ratio can be used to determine the number of layer. Nonetheless, single layer graphene films grown on Cu foil are expected to have 1-3 layers with the high probability of 1 layer mostly covering the target sample. In general, when the above peak ratio is less than 1 it corresponds to 1 layer. However, peak ratio of I(G)/I(2D) = 1 stands for bilayer graphene and for ratios more than 1, the number of layer is predicted to be 3 or more (as in multilayer graphene). Based on the Raman data extracted from our samples, the substrate is mostly covered by 1 layer of graphene with few area having 2 or 3 layers. Figure 4.2 shows the Raman spectrum for SLG and MLG samples for different locations on the sample.

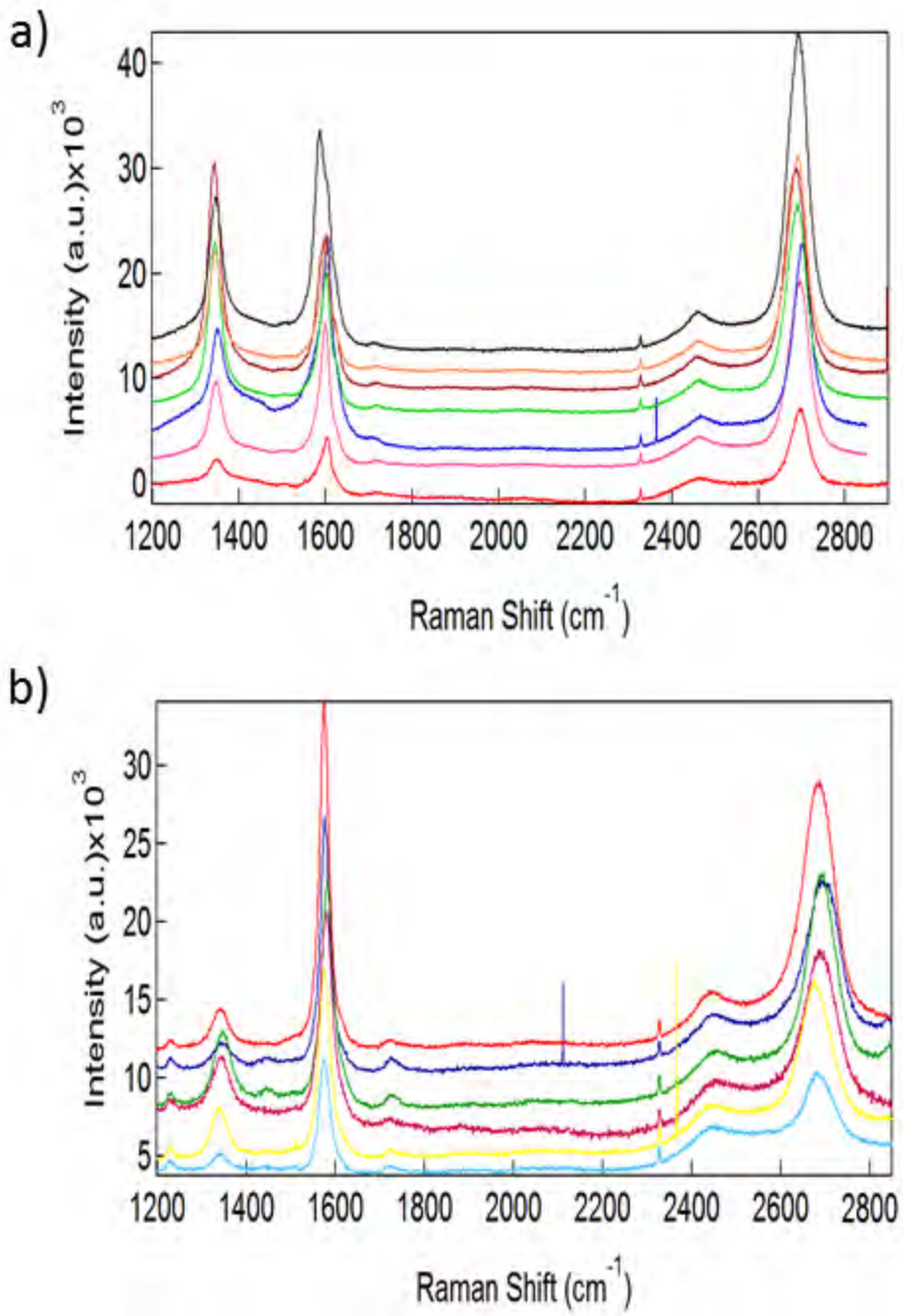

Figure 4.2. Raman spectrum of transferred single layer (a) and multi layer (b) graphene to calculate the ratio of G to 2D peak. Curves are shown with offset shifts to enhance clarity.

4.2.3. SUBSTRATE PREPARATION

Two different approaches were selected for this part. First was to fabricate perpendicular microfluidics with a graphene membrane in between. This is designed to be done on SiO_2 substrate. The second structure involves puncturing holes (5x5 μm, 10x10 μm, 20x20 μm, and 30x30 μm, each set in one quadrant of wafer) on the suspended silicon-nitride membrane on silicon wafer. Next, graphene film will be transferred on top of that hole (covering it completely) making a square graphene membrane with different sizes. Both these designs are shown in Figure 4.3.

4.2.3.1. Microfluidic channels and graphene

In the first attempt to suspend graphene we tried the perpendicular microfluidic channels with graphene film in between. Silicon wafers with 300 nm dry oxide was used. The bottom channels (5 parallel channels of 5 μm width, and ~1 cm length with ~50 μm pitch) were patterned and the SiO_2 was dry etched using Trion (RIE) machine. The parameters to etch SiO_2 are as follows: RIE power of 100 W, O_2 and CH_4 gas flows of 5 sccm and 45 sccm respectively. The process time is 15 minutes and chamber pressure was set to 150 mTorr. Samples were then put in STS machine to etch the silicon in order to make deeper channels for liquid to flow easier. STS was set on "Processb" for 15 minute/43 cycles (etches ~50 μm of silicon). In all above steps the photoresist (used to pattern oxide at the first step) was kept since STS can easily etch oxide too (although with lower rate comparing to silicon). Sample is then dipped in Acetone to remove the photoresist. To get rid of the residue of photoresist we used Gasonic machine (oxygen asher) for 3-5 minutes at 90-150 ^oC with plasma power of 1100 W and chamber pressure 3000 mTorr.

After that, graphene samples were transferred on top of the channels (transfer process is discussed in the next section).

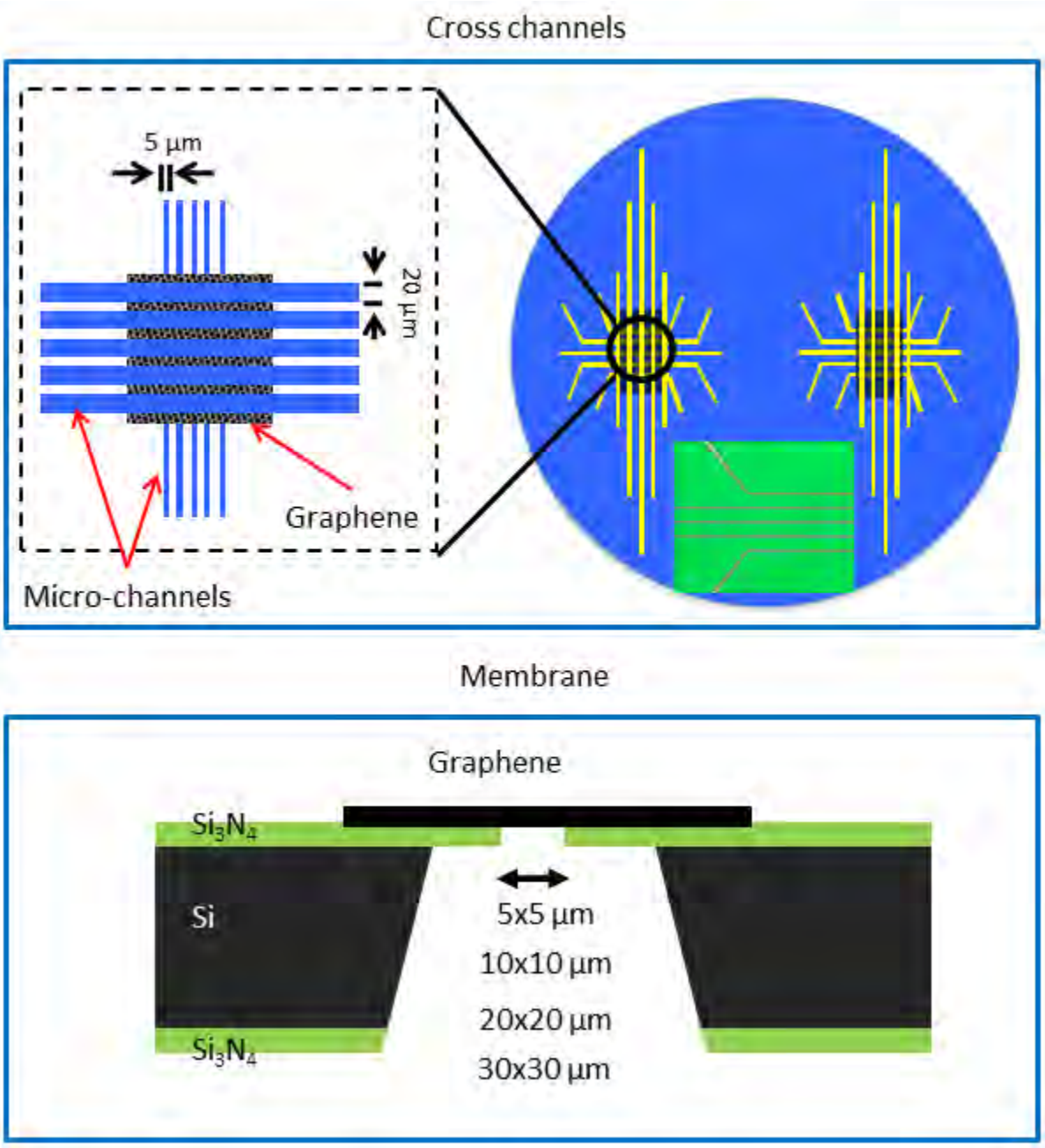

Figure 4.3. different designs to make suspended graphene membrane.

Since the channel length is in the range of centimeter, single layer graphene could not cover the channels and would break easily during the transfer process. In contrast, multilayer graphene could partly cover some areas of the channels but they would also break in the next step which is the formation of the top channel (perpendicular to the bottom channel).

Top microchannels are made of PDMS with 20 μm width, ~50 μm depth, and ~1 cm length. First, SU8-50 molds were made on top of bare silicon wafer. Silicon wafer is treated with Piranha (3:1, sulfuric acid : hydrogen peroxide) for 60 minutes at 120 ^{o}C and rinsed in DI water (5 minutes). Then wafer is put in dehydration oven (120 ^{o}C) for 30 minutes followed by spin-coating of SU8. The tricky part was pouring SU8 (not squeezing the bottle) so that no (or very few) bubbles are in the thick film, covering 60-70% of the wafer area. Spinning parameters are, 500 rpm for 10 sec (100 rpm/s) followed by 2500 rpm for 30 sec (300 rpm/s). Soft bake is done on hot plate starting from room temperature (R.T.) and slowly ramping up the temperature to 65 ^{o}C and wait for 6 minutes, subsequently, ramping at 10 ^{o}C to reach 95 ^{o}C and wait for another 20 minutes. The gradual increase in the temperature prevents the film from cracking and introduces less stress. Then samples are removed from hot plate and left for 20 min to cool down slowly. Exposure using the mask is done in UV (200 mJ/cm^2). Post bake is also done on hot plate at 65 ^{o}C for 1 min and 95 ^{o}C for 5 min ramping at 10 ^{o}C/min for both parts followed by 20 min cooling down in room temperature. The area exposed to UV will be hardened while the rest of SU8 will be developed using the recommended SU8 developer. The sample is put in the developer and every 30 sec it should be taken out of the solution for 1-3 sec. This continues for about 5 minutes (depending on how strong the developer is, since sometime the used and new developers can be mixed). At the end, rinse the samples with fresh developer for 10 sec and rinse with IPA thoroughly. Do NOT use DI water in any step and after the mold was prepared, this

will make SU8 mold to peel off of the silicon wafer. It is also worth to mention that SU8 mold cannot be made on SiO_2 substrate because of weak bonding to the oxide surface. Oxygen plasma can also be used to clean the SU8 residues at the end of the process. The final SU8 mold will be ~50 μm thick (since we used SU8-50), which defines the depth of PDMS channel.

Now that SU8 mold is ready, we can cast the PDMS channel. Sample (mold) is washed with IPA (NO water at all) and dried completely. PDMS mixed is prepared in plastic pouch using Silicone and curing agent (10:1, weight (silicone) : mL (curing agent), e.g. 10 gr of silicone with 1 mL of agent gives ~1-2 mm thick PDMS covering a 4" wafer). Pouch is sealed and the solution should be mixed completely. The bag is then put in degas vacuum chamber to remove the bubbles made during shaking process (~30 min). Few drops of Sigmacote (from Sigma Aldrich) were poured on SU8 mold covering the whole area and the sample was dried out completely. Sigmacote prevents the PDMS solution to stick on the surface. After drying the sample/sigmacote, PDMS mixture is poured carefully on the mold so that no bubble is created. Next, sample can be put in the oven or on hot plate until the PDMS is cured. Then, the final PDMS with microfluidic channels embedded in it can be peeled off of the mold and is ready to be put on top of the channel (made in wafer)/graphene (transferred on channel).

As described, the process environment towards the end was too harsh for graphene films to survive since along one direction (parallel to the bottom channel), graphene sheet will be suspended all long and that causes a lot of stress on the film which eventually breaks the film. Figure 4.4 shows the process steps and optical image results of the transferred graphene films. Although, as shown, for multilayer graphene samples, graphene sheets will cover the bottom channel but as soon as the top channel are put on top or the liquid flows inside the channel these

films will also break. Single-layer graphene sheets are very fragile and break over the bottom channel during the transfer.

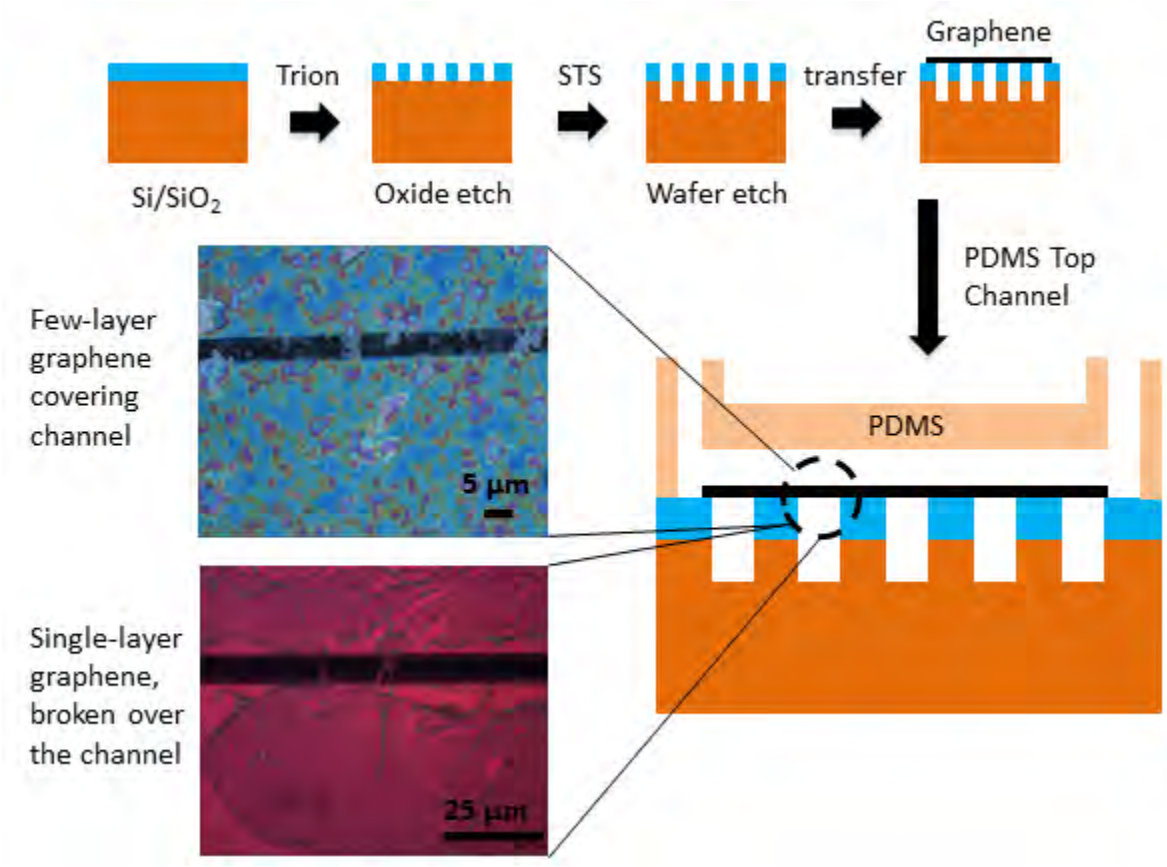

Figure 4.4. Fabrication process for microfluidic channels design. Optical images show MLG covering the bottom channel but breaks after putting the top channel. On the other hand, SLG film breaks over the bottom channel during transfer process as shown in the image (lower one).

4.2.3.2. Graphene membrane on silicon-nitride

Silicon-nitride is known as an etch stop to silicon wafer in KOH wet etching process. Therefore, it is well-established to prepare silicon-nitride membrane on top of silicon wafer by wet etching the wafer in KOH all the way to the nitride cap. It should be noted that KOH etching of silicon is anisotropic and results in V shape walls. Silicon wafers with 300 nm low-stress LPCVD SiN on both sides were bought. The back side of the wafer was patterned using Shipley

1827 photoresists (same method as described in chapter 3, fabrication section). The fabrication steps are shown in Figure 4.5.

Before etching the silicon substrate, the patterned nitride on the back side of the wafer (circles of 1 mm diameter with the pitch of 1 cm from center-to-center) should be removed to open a window. Trion (RIE) machine is used for this purpose with the following settings: O_2 and CH_4 gases used with the flow of 5 sccm and 45 sccm respectively. The chamber pressure is set to 150 mTorr and plasma power is 100 W. To make sure that nitride is etched completely the run time was set to 7-10 minutes. Top holes (5x5 μm to 30x30μm) were also patterned subsequently by using PMGI/Shipley 1827 PRs and back-side alignment technique (using MA-6) to align them in the middle of the final nitride membrane (which will be formed after silicon wet etching). Then photoresist is removed and sample is put in KOH for wet etching of silicon substrate from back to the top side leaving the nitride membrane (with hole in the middle) on the top. 100 mg of KOH was dissolved in 200 mL DI water and heated up to 80 ^{o}C (with a lid on the beaker). Sample was put in the solution and left overnight (~18 hours) until the wafer is completely etched to the top. Next, sample was washed and dried thoroughly. Now the substrate is ready to transfer graphene on top of the nitride membrane with the hole. The purpose is to cover the hole with graphene. Single and few layer graphene films were used and the process is described in the next section.

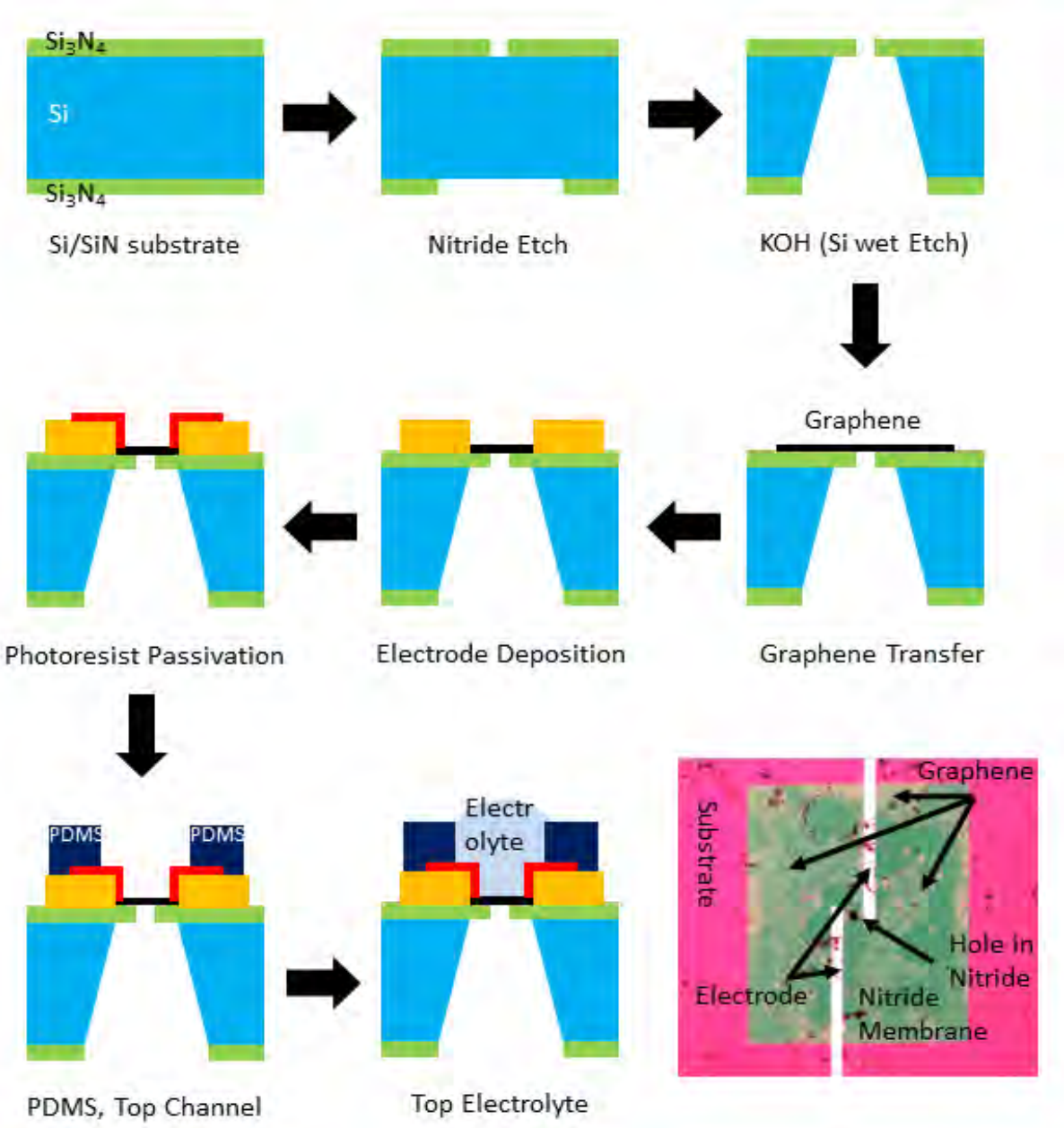

Figure 4.5. Fabrication steps' schematic to make suspended graphene membrane over square holes patterned on silicon-nitride membrane. Last figure shows the optical image of one fabricated membrane, pink is substrate (Si/SiN), green part is the nitride membrane and the graphene patches are also shown. Two electrode fingers with the hole in the membrane (covered by graphene) in between is pointed out in the figure.

4.2.4. GRAPHENE TRANSFER

Graphene, as mentioned, is provided by outside supplier (2"x2" CVD grown single layer graphene on Cu foil). The objective is to etch Cu foil and transfer graphene to any arbitrary substrate. Poly-methyl methacrylate (PMMA) is used to cover one side of the foil to hold graphene while the Cu foil is being etched. PMMA powder (9 gr) is dissolved in 100 mL of Chlorobenzene (99.8% purity, density = 1.107) and mixed well. It should be left for 3 days for the PMMA to completely dissolve in the solution and result in 9% PMMA solution. Next, some droplets of PMMA were poured on the foil and spin-coated at 4000 rpm for 50-60 sec. Cu/graphene/PMMA is then put on hot plate at 195 ^{o}C for curing. $FeCl_3$ (0.5 M or 1M) solution is used to etch the Cu foil leaving the graphene/PMMA floating on the surface of etchant. Etch time varies from 30-120 minutes until visually no Cu is attached to the graphene/PMMA film. Following that, samples are put in DI water (changing every few hours until the water's color is clear) to get rid of etchant residues. Now the film is ready to be transferred onto the prepared substrate (nitride membrane with hole). To make sure of better transfer of graphene we use double-PMMA method as described in [25]. After transferring on top of substrate, few droplets of PMMA were put on the sample covering the graphene/PMMA film and wait for 30-60 min for PMMA to dry out. Later, the sample is put in Acetone to dissolve PMMA.

4.2.5. TRANSISTOR WITH TOP ELECTROLYTE GATE

4.2.5.1. Design flaw and solution

Now that we are able to fabricate suspended graphene membrane, we came to the idea of gating it with electrolyte and study the response. The problem is that electrode deposition and PDMS/electrolyte set up on top of graphene membrane all introduce stress to the graphene film

which will eventually break the membrane (especially for single layer graphene and bigger hole sizes). Therefore we decided to redesign the fabrication part. The first source of pressure to membrane is from Acetone when dipping the sample to remove PMMA. Immersing and taking out the sample both can cause cracks in graphene membrane so this step should be replaced by a dry process. Recently annealing was suggested as an alternative to the Acetone removal of PMMA [26-29]. Here we studied annealing to come up with the appropriate recipe to remove the PMMA. Annealing is done in forming gas (5-10% H_2 and 95-90% Ar) at 400 ^oC for 3 hours (atmospheric pressure). Results show clean sample with slight change in Raman spectrum of the film. Figure 4.6 shows the annealing process and Raman data as well as the optical images before and after 3 hours annealing. It can be seen that there is no trace of PMMA after annealing.

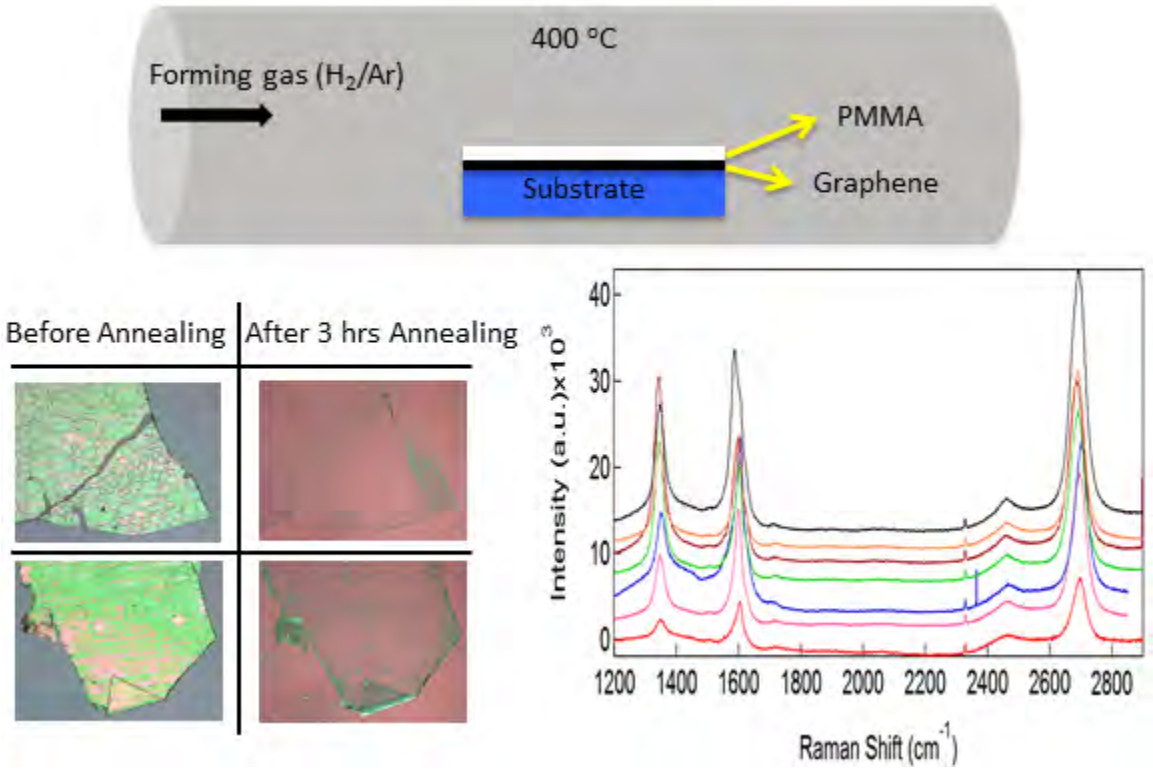

Figure 4.6. Annealing process and Raman spectrum of SLG after anneal (curves are shifted with constant offset for clarity). Images show before (left) and after 3 hours annealing (right) at the same spot showing the cleaned graphene without PMMA residue.

For single layer graphene it was observed that the Raman for G peak (average) was shifted by 4.6 cm^{-1} and 2D peak (average) is shifted by 3.2 cm^{-1}. This is in consistent with the recent results published at the same time (our data is unpublished) [30].

4.2.5.2. Post-transfer process

Next step is the electrode fingers deposition. Conventional photolithography was used with PMGI/Shipley 1827 photoresists to make precise alignment to the membrane holes. Since the patterning, development, and lift off process involves several wet chemistry, it is recommended to dip the substrate vertically into any solution so that the graphene membrane would not break. E-beam deposition is used to deposit Palladium/Gold (10/40 nm) electrodes followed by lift off in Nano-remover as explained in chapter 3 (fabrication section). The channel length and width vary for different devices with different hole sizes. The range starts with 15x10 μm (LxW) for 5x5 μm hole and goes up to 20x20 μm, 40x30 μm, and 50x40 μm for other hole sizes respectively. Following the deposition, electrodes were passivated to prevent the leakage current between electrodes and the top electrolyte in the microchannel. The passivation is also done by PMGI/Shipley 1827 followed by post-bake to ensure good adhesion quality of the photoresists.

To design the microfluidic channel, after several attempts it was observed that the best choice is to individually access each device. PDMS microfluidic channels with different width from 400 μm up to 1 mm were designed and casted using the procedure mentioned earlier. The advantage of individually controlling the devices is the microchannel cleaning issue and also if one membrane breaks it would not affect the adjacent devices' performance. Figure 4.7 shows the top-view design and the top microfluidic channel used for devices.

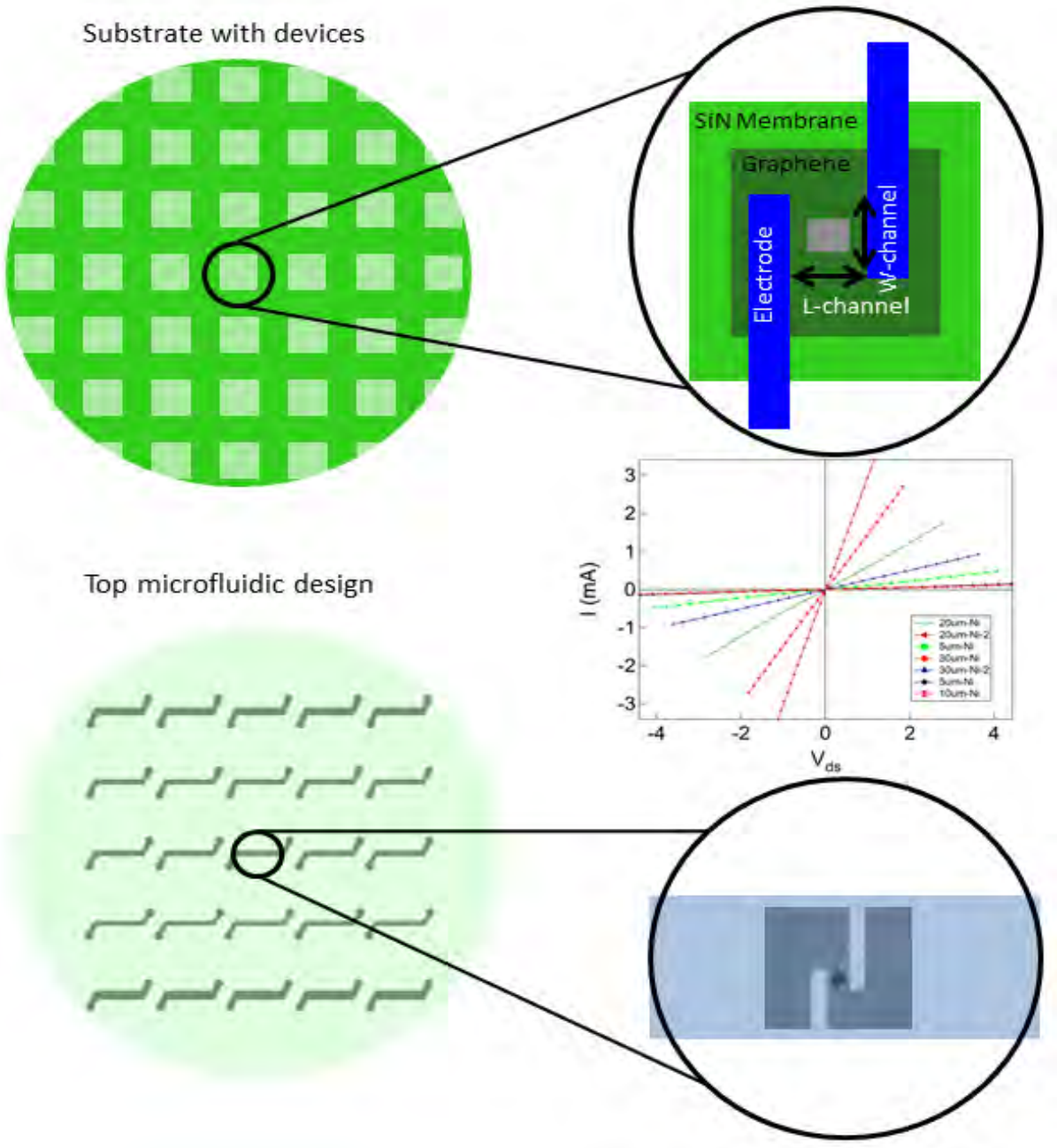

Figure 4.7. Top-veiw of device channel with different length and width design and top PDMS microfluidic channel. Electrical results from multi-layer graphene films (NOT gated) with different channel lengths and widths.

As shown here, the electrodes are designed so that the channel length and width is independent of graphene film's area since the two electrodes only overlap for the channel width

section and each of them is connected to the next top (or bottom) device. Not only it makes each device independent of graphene film size, but also it makes it possible for studying the basic logic circuit (i.e. inverters) without any change in the design (this is discussed in "Future Proposal" section).

4.2.5.3. Electrical measurement

So far, fabrication methods used to make freely suspended graphene membrane was shown. Single layer and few layer graphene films were deposited on the substrate at different hole sizes. Figure 4.7 demonstrates the suspended graphene samples. The difference in the I-V slope (resistance) comes from the difference in number of graphene layer as well as the channel length to width ratio.

Additionally, we tried the liquid gated graphene samples (Figure 4.8). Since the process design was not optimized until recently, there is not much of data available. It is worth to mention that the primary objective of this project was merely fabricating suspended graphene. The main issue with electrolyte-gated devices was gate leakage current. Partly it was due to the weak passivation layer. After putting the top PDMS microfluidic channel it was seen that in some devices it can scratch the passivation layer (due to movement of PDMS on the substrate during visual alignment to the hole/graphene area). The individual microchannel also helped eliminating this problem.

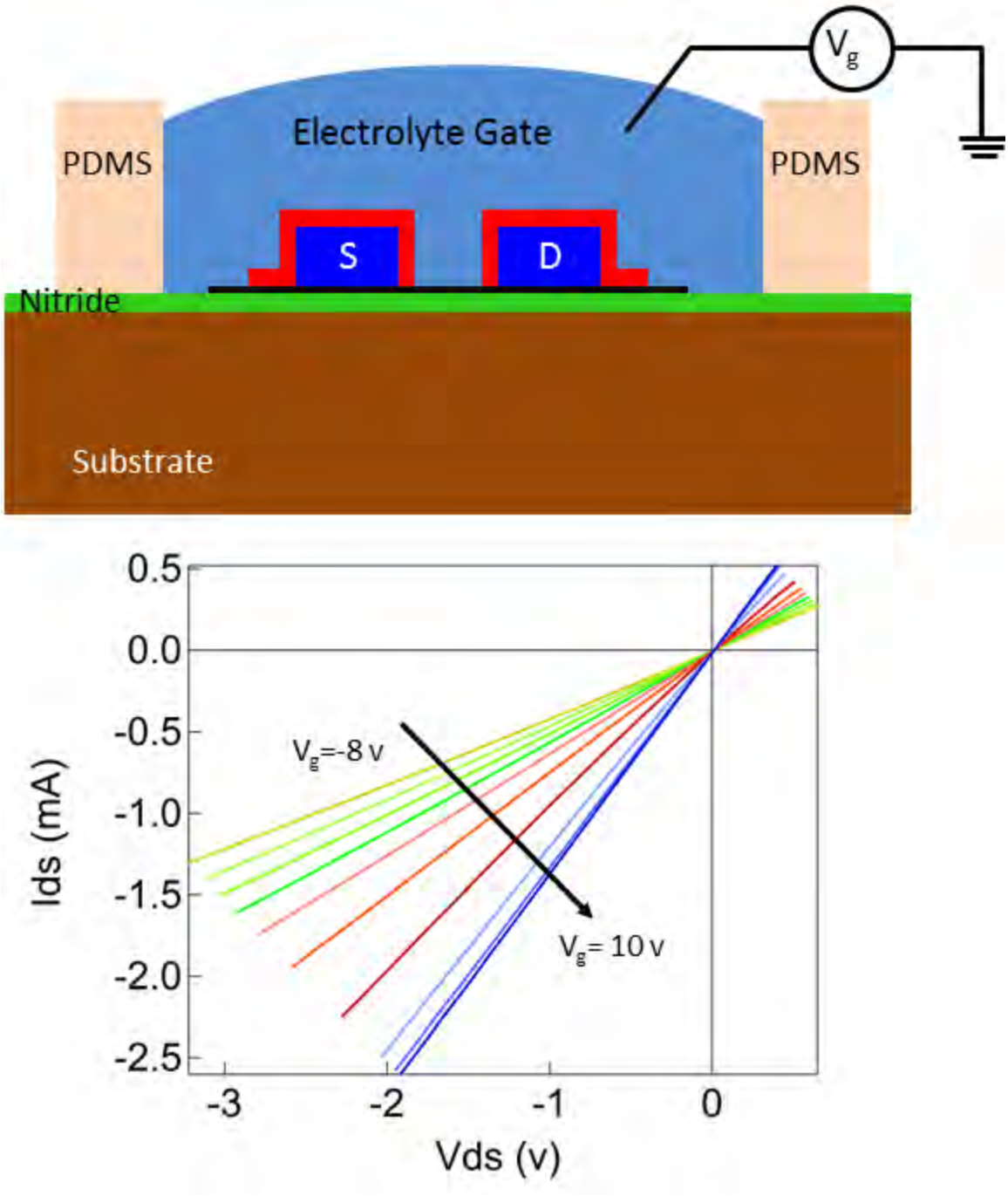

Figure 4.8. Top-electrolyte gate set up (top). Electrical data from measurement with V_g going from -8 V to 10 V (bottom). Measurement is done on single layer graphene.

For measuring the liquid-gated graphene device, we transferred single layer graphene on top of Si/SiN substrate (not the suspended membrane, as shown in Figure 4.8). Then deposited and

passivated electrodes to put the microchannel on top. For the electrolyte we used 10 mM NaCl. Channel length is 15 μm and channel width is 10 μm. Gate leakage current in this device was 2-8% of the source-drain current which is typical in electrolyte gated graphene based devices. Gate voltage changes from -8 V to 10 V with 2 V increments. We were able to see the gating effect on SLG using electrolyte gate. The result is shows in Figure 4.8. It can be seen that by increasing the gate voltage, the resistance decreases but we were not able to reach the minimum conductance point (also known as, *Dirac* point).

4.3. CONCLUSION

In conclusion, we developed methods for integration of a freely suspended graphene membrane into a microfluidic chamber. We tried to have two microfluidic channels: One above the free suspended graphene membrane, and the other beneath the freely suspended graphene membrane. This failed, as there were too many process steps that could go wrong. Instead, we developed a process where we transferred graphene as a free standing membrane on a square hole of different sizes. In this work, the primary challenge was that graphene would crack after the membrane was transferred, especially for large size holes. To solve this issue we developed the protocol to remove the PMMA (and other residues) using annealing in forming gas instead of Acetone. As a result, we were able to transfer graphene to up to 30x30 μm holes as free standing membranes. We also found that removing PMMA (using annealing technique) will result in slight shift in G (4.6 cm^{-1} shift) and 2D peaks (3.2 cm^{-1} shift) of the same sample.

Establishing the above design and fabrication processes, we measured electrical characteristic of different membrane sizes for MLG. Basically, there are a lot of parameters for

MLG such as number of layers and the contact resistance that affects the response of the devices therefore we couldn't establish a trend for this device. On the other hand, we studied the electrolyte gated graphene transistor. Generally, we observed the gating effect as shown in Figure 4.8. It can be seen that by increasing the gate voltage, the resistance decreases.

4.4. FUTURE PROPOSALS

There are many directions for the future of this project:

- LPCVD furnace for single layer graphene synthesize (on Cu foil)
- Dielectric development
- Graphene + Ebeam lithography quantum dots
- THz graphene/nanotube based quantum dot detectors
- Aperture work: THz transmission through pinhole in graphene membrane?
- Dual-electrolyte gated graphene membrane (top and bottom electrolyte)
- Lipid bilayer/graphene biosensor
- Graphene Nanopore
- DNA sequencing using graphene nanopore

The aperture work seemed interesting, because graphene can guide THz light therefore, I started to lead that project in the meantime. The data is not properly processed and therefore is not presented here. Generally, it may be possible to integrate graphene into being both the detector and the waveguide/aperture/antenna to focus the THz light on. This is an unclear concept at the moment but the basic ingredients have already been obtained in our lab.

The other possible option is to develop a *Graphene electrochemistry platform: Transport, fluidics, lipid bilayer/graphene interaction and nanopore integration.* This idea is shown schematically in the figure below. Based on our initial work we have shown the feasibility, but it would take one or two grad student years to fully implement that.

Meanwhile, the electrode fingers design in my masks makes it possible to investigate the output characteristic of top-electrolyte-gated graphene-based inverters as shown here.

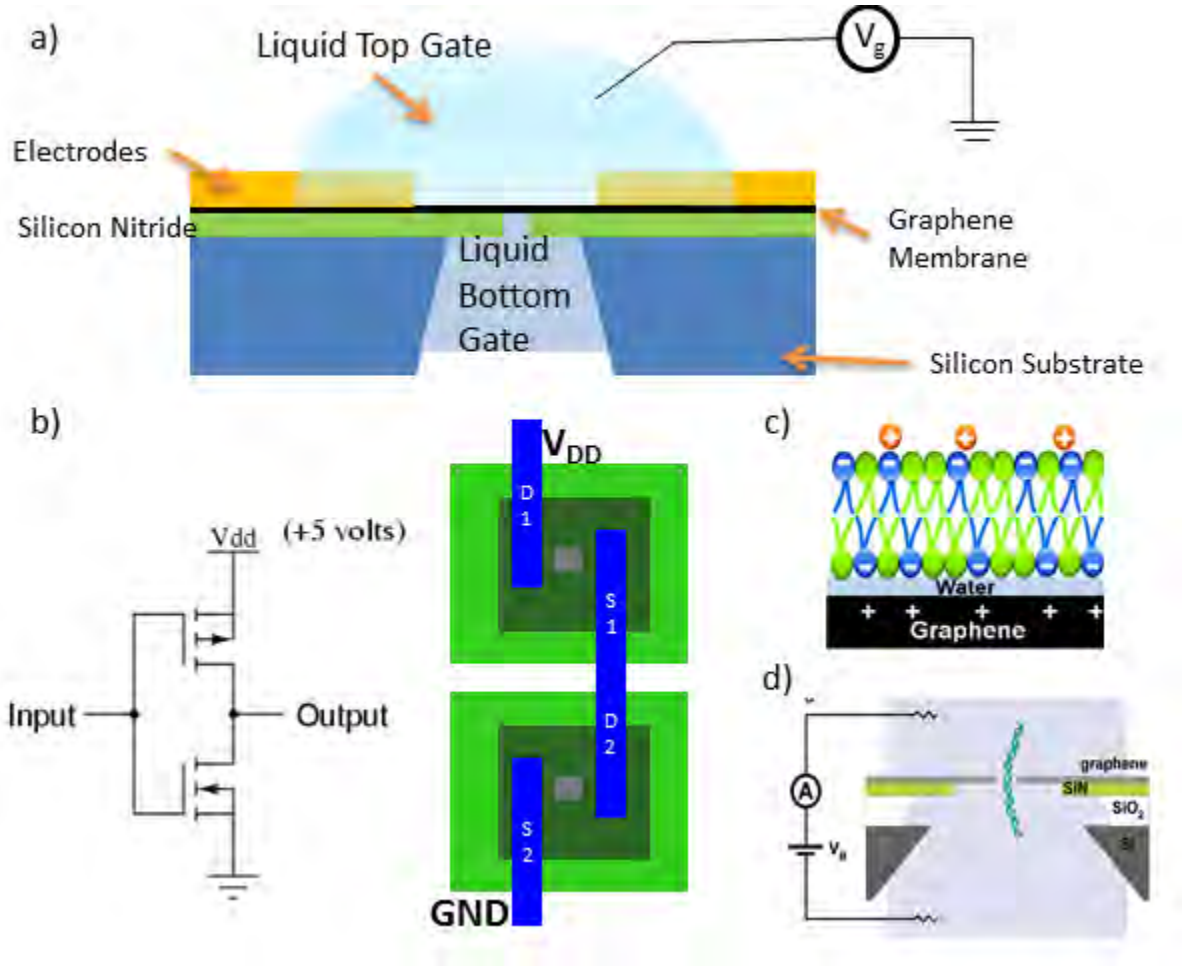

Figure 4.9. Proposed future works. a) Dual-electrolyte-gates suspended graphene transistors. b) Electroly-gated graphene based inverters. c) Lipid bilayer/graphene structure [31]. d) Graphene Nanopore and DNA sequencing through graphene nanopore [32].

4.5. ACKNOWLEDGMENT

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4.6. REFERENCES AND NOTES

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science,* vol. 306, pp. 666-669, Oct 22 2004.

[2] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature Materials,* vol. 6, pp. 183-191, Mar 2007.

[3] T. Ohta, A. Bostwick, T. Seyller, K. Horn, and E. Rotenberg, "Controlling the electronic structure of bilayer graphene," *Science,* vol. 313, pp. 951-954, Aug 18 2006.

[4] B. Ozyilmaz, P. Jarillo-Herrero, D. Efetov, and P. Kim, "Electronic transport in locally gated graphene nanoconstrictions," *Applied Physics Letters,* vol. 91, Nov 5 2007.

[5] Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H. Y. Chiu, A. Grill, and P. Avouris, "100-GHz Transistors from Wafer-Scale Epitaxial Graphene," *Science,* vol. 327, pp. 662-662, Feb 5 2010.

[6] J. S. Bunch, S. S. Verbridge, J. S. Alden, A. M. van der Zande, J. M. Parpia, H. G. Craighead, and P. L. McEuen, "Impermeable atomic membranes from graphene sheets," *Nano Letters,* vol. 8, pp. 2458-2462, Aug 2008.

[7] C. Y. Chen, S. Rosenblatt, K. I. Bolotin, W. Kalb, P. Kim, I. Kymissis, H. L. Stormer, T. F. Heinz, and J. Hone, "Performance of monolayer graphene nanomechanical resonators with electrical readout," *Nature Nanotechnology,* vol. 4, pp. 861-867, Dec 2009.

[8] S. Shivaraman, R. A. Barton, X. Yu, J. Alden, L. Herman, M. V. S. Chandrashekhar, J. Park, P. L. McEuen, J. M. Parpia, H. G. Craighead, and M. G. Spencer, "Free-Standing Epitaxial Graphene," *Nano Letters,* vol. 9, pp. 3100-3105, Sep 2009.

[9] A. Reina, X. T. Jia, J. Ho, D. Nezich, H. B. Son, V. Bulovic, M. S. Dresselhaus, and J. Kong, "Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition," *Nano Letters,* vol. 9, pp. 30-35, Jan 2009.

[10] X. S. Li, W. W. Cai, J. H. An, S. Kim, J. Nah, D. X. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, "Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils," *Science,* vol. 324, pp. 1312-1314, Jun 5 2009.

[11] C. Mattevi, H. Kim, and M. Chhowalla, "A review of chemical vapour deposition of graphene on copper," *Journal of Materials Chemistry,* vol. 21, pp. 3324-3334, 2011.

[12] C. Berger, Z. M. Song, X. B. Li, X. S. Wu, N. Brown, C. Naud, D. Mayou, T. B. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, and W. A. de Heer, "Electronic confinement and coherence in patterned epitaxial graphene," *Science,* vol. 312, pp. 1191-1196, May 26 2006.

[13] P. Sutter, "EPITAXIAL GRAPHENE How silicon leaves the scene," *Nature Materials,* vol. 8, pp. 171-172, Mar 2009.

[14] L. Y. Jiao, L. Zhang, X. R. Wang, G. Diankov, and H. J. Dai, "Narrow graphene nanoribbons from carbon nanotubes," *Nature,* vol. 458, pp. 877-880, Apr 16 2009.

[15] D. V. Kosynkin, A. L. Higginbotham, A. Sinitskii, J. R. Lomeda, A. Dimiev, B. K. Price, and J. M. Tour, "Longitudinal unzipping of carbon nanotubes to form graphene nanoribbons," *Nature,* vol. 458, pp. 872-U5, Apr 16 2009.

[16] V. C. Tung, M. J. Allen, Y. Yang, and R. B. Kaner, "High-throughput solution processing of large-scale graphene," *Nature Nanotechnology,* vol. 4, pp. 25-29, Jan 2009.

[17] M. Choucair, P. Thordarson, and J. A. Stride, "Gram-scale production of graphene based on solvothermal synthesis and sonication," *Nature Nanotechnology,* vol. 4, pp. 30-33, Jan 2009.

[18] S. V. Morozov, K. S. Novoselov, M. I. Katsnelson, F. Schedin, D. C. Elias, J. A. Jaszczak, and A. K. Geim, "Giant intrinsic carrier mobilities in graphene and its bilayer," *Physical Review Letters,* vol. 100, Jan 11 2008.

[19] A. Akturk and N. Goldsman, "Electron transport and full-band electron-phonon interactions in graphene," *Journal of Applied Physics,* vol. 103, Mar 1 2008.

[20] P. Blake, E. W. Hill, A. H. C. Neto, K. S. Novoselov, D. Jiang, R. Yang, T. J. Booth, and A. K. Geim, "Making graphene visible," *Applied Physics Letters,* vol. 91, Aug 6 2007.

[21] Y. K. Koh, M. H. Bae, D. G. Cahill, and E. Pop, "Reliably Counting Atomic Planes of Few-Layer Graphene (n > 4)," *Acs Nano,* vol. 5, pp. 269-274, Jan 2011.

[22] S. P. Koenig, N. G. Boddeti, M. L. Dunn, and J. S. Bunch, "Ultrastrong adhesion of graphene membranes," *Nature Nanotechnology,* vol. 6, pp. 543-546, Sep 2011.

[23] Z. H. Ni, H. M. Wang, J. Kasim, H. M. Fan, T. Yu, Y. H. Wu, Y. P. Feng, and Z. X. Shen, "Graphene thickness determination using reflection and contrast spectroscopy," *Nano Letters,* vol. 7, pp. 2758-2763, Sep 2007.

[24] D. Graf, F. Molitor, K. Ensslin, C. Stampfer, A. Jungen, C. Hierold, and L. Wirtz, "Spatially resolved raman spectroscopy of single- and few-layer graphene," *Nano Letters,* vol. 7, pp. 238-242, Feb 2007.

[25] X. S. Li, Y. W. Zhu, W. W. Cai, M. Borysiak, B. Y. Han, D. Chen, R. D. Piner, L. Colombo, and R. S. Ruoff, "Transfer of Large-Area Graphene Films for High-Performance Transparent Conductive Electrodes," *Nano Letters,* vol. 9, pp. 4359-4363, Dec 2009.

[26] A. S. Mayorov, R. V. Gorbachev, S. V. Morozov, L. Britnell, R. Jalil, L. A. Ponomarenko, P. Blake, K. S. Novoselov, K. Watanabe, T. Taniguchi, and A. K. Geim, "Micrometer-Scale Ballistic Transport in Encapsulated Graphene at Room Temperature," *Nano Letters,* vol. 11, pp. 2396-2399, Jun 2011.

[27] E. Stolyarova, K. T. Rim, S. M. Ryu, J. Maultzsch, P. Kim, L. E. Brus, T. F. Heinz, M. S. Hybertsen, and G. W. Flynn, "High-resolution scanning tunneling microscopy imaging of mesoscopic graphene sheets on an insulating surface," *Proceedings of the National Academy of Sciences of the United States of America,* vol. 104, pp. 9209-9212, May 29 2007.

[28] M. Ishigami, J. H. Chen, W. G. Cullen, M. S. Fuhrer, and E. D. Williams, "Atomic structure of graphene on SiO2," *Nano Letters,* vol. 7, pp. 1643-1648, Jun 2007.

[29] J. L. Xia, F. Chen, J. H. Li, and N. J. Tao, "Measurement of the quantum capacitance of graphene," *Nature Nanotechnology,* vol. 4, pp. 505-509, Aug 2009.

[30] A. Pirkle, J. Chan, A. Venugopal, D. Hinojos, C. W. Magnuson, S. McDonnell, L. Colombo, E. M. Vogel, R. S. Ruoff, and R. M. Wallace, "The effect of chemical residues on the physical and electrical properties of chemical vapor deposited graphene " *Applied Physics Letters,* vol. 99, p. 122108, 2011.

[31] P. K. Ang, M. Jaiswal, C. H. Y. X. Lim, Y. Wang, J. Sankaran, A. Li, C. T. Lim, T. Wohland, O. Barbaros, and K. P. Loh, "A Bioelectronic Platform Using a Graphene-Lipid Bilayer Interface," *Acs Nano,* vol. 4, pp. 7387-7394, Dec 2010.

[32] C. A. Merchant, K. Healy, M. Wanunu, V. Ray, N. Peterman, J. Bartel, M. D. Fischbein, K. Venta, Z. T. Luo, A. T. C. Johnson, and M. Drndic, "DNA Translocation through Graphene Nanopores," *Nano Letters,* vol. 10, pp. 2915-2921, Aug 2010.

CHAPTER FIVE

SUMMARY AND CONCLUSION

5.1. SUMMARY OF FINDINGS AND CONCLUSION

Carbon based materials (carbon nanotubes, graphene, etc.) are demonstrating a great promising future to be embedded in electronic device technology. However, scalable, high-performance techniques are needed before commercializing these exotic materials. Moreover, strong theoretical studies of such devices is lacking in many aspects. It was the main goal of this thesis research to experimentally explore some of these unknowns which in some cases seem to be hardly approachable theoretically.

Electronic devices and sensors based on carbon nanotube and graphene have been studied in detail here. Different deposition and fabrication techniques were explored for carbon nantubes to realize the impact of different parameters on devices' output performance. Furthermore, graphene transfer technology and fabrication of suspended graphene membrane has been researched resulting in high yield, wafer-scale suspended single and multi-layer graphene films.

Carbon nanotube ink consisting mixture of metallic and semiconducting tubes dispersed in the solution is studied. Dielectrophoretic force was applied to make dense, and aligned network of nanotubes in desired location on the wafer. The effect of 3 major surfactants and also different DEP deposition conditions (voltage and frequency ranges) were explained. Using DEP, the alignment was found to be very perfect for the optimum condition. However, it was noticed that DEP mainly results in deposition of metallic tubes (low on/off ratio) which will be helpful for low-resistivity connection pathways (such as 50 Ohms matching circuit), vias, and interconnect applications but not field effect transistors in which the channel is supposed to be controlled by applied gate voltage. Although the technique results in aligned network, it is not yet scalable since each device should be DEP treated individually.

In contrast, another approach was designed to utilize purified semiconducting nanotube ink (> 90% semiconducting) to fabricate printed carbon nanotube-based transistors. As the main objective, we tried to study the impact of several parameters on the output characteristic of thin film transistors made from purified nanotube ink as the base material. Among all the suggested parameters, it was observed that network density plays a major role in controlling the devices' output. A new deposition technique was employed to change the density of the network. Finally, we were able to lay down nanotube network of 99% semiconducting material with a broad range of densities from 10 tubes/μm^2 up to 100 tubes/μm^2 using and original ink's density variation as well as surface modification. A comprehensive range of mobilities from 5 cm^2/V-s up to ~100 cm^2/V-s (close to that of p-type silicon technology) with on/off ratio from 10 to more than 10^5 was obtained with this technique. Based on this, we established a relationship between mobility and on/off ratio with regard to density of the network. It has been shown that there exist a strong correlation between on/off ratio and mobility and density of nanotubes. Nonetheless, the theoretical background of such experimental understanding is lacking so far.

Besides carbon nanotubes, graphene was also considered as an atomic-thin suspended layer. High yield, wafer-scale fabrication method was developed to make suspended graphene films on the desired locations. Primary results show a high yield of single and multi-layer nanotubes covering holes of 5x5 μm up to 30x30 μm with changing sheet resistivity based on membrane size (i.e. aspect ratio). Also the electrical measurements show gating effect of graphene samples using electrolyte as the gate. Future investigations include making nano-size pores on this membrane and use this as nanopore for biosensing and DNA sequencing.

In addition to all above, we are currently working on the graphene broadband sheet conductivity from DC to THz in collaboration with University of Barcelona and Wright State University. We were able to measure, for the first time, the sheet resistance of both single and multi-layer graphene samples in a broadband up to 1 THz. The results are currently being processed. Unfortunately since the final results have not yet been processes to the high standards, they are not presented here.

In sum, nanotube based semiconducting ink has been demonstrated to be technically superior in terms of mobility to any other semiconducting ink. This work lays a clear roadmap for the applications of nanotube based semiconducting inks in printed electronic. Practitioners and circuit designers can now quantitatively study the tradeoff between mobility and on/off ratio in systems design, and adjust the nanotube density for optimum system performance. Prior to our studies, this was done on a hit/miss type basis. It is highly anticipated that purified semiconducting nanotube ink would find applications in electronics, especially the printed electronics which seems to be low-hanging fruit. Furthermore, the graphene membrane fabrication technique developed here is demonstrating high yield, large-scale suspended membranes of graphene on the wafer. This opens up new windows for future graphene membrane researches including “dual-electrolyte-gated graphene membrane transistors”, “lipid bilayer/suspended graphene interaction”, “graphene nanopores for DNA sequencing”, etc.

Appendix: Probe Station and Measurement Set-up