nature nanotechnology

REVIEW ARTICLE

PUBLISHED ONLINE: 29 NOVEMBER 2009 | DOI: 10.1038/NNANO.2009.355

Nanotube electronics for radiofrequency applications

Chris Rutherglen, Dheeraj Jain and Peter Burke*

Electronic devices based on carbon nanotubes are among the candidates to eventually replace silicon-based devices for logic applications. Before then, however, nanotube-based radiofrequency transistors could become competitive for high-performance analogue components such as low-noise amplifiers and power amplifiers in wireless systems. Single-walled nanotubes are well suited for use in radiofrequency transistors because they demonstrate near-ballistic electron transport and are expected to have high cut-off frequencies. To achieve the best possible performance it is necessary to use dense arrays of semiconducting nanotubes with good alignment between the nanotubes, but techniques that can economically manufacture such arrays are needed to realize this potential. Here we review progress towards nanotube electronics for radiofrequency applications in terms of device physics, circuit design and the manufacturing challenges.

The potential to exploit single-walled carbon nanotubes in advanced electronics has been a major goal in nanotechnology for over a decade[1,2]. This interest stems from the fact that carbon nanotubes offer a combination of small size, high mobility[3,4], large current density and low intrinsic capacitance: moreover, their intrinsic cut-off frequency is expected to be high. Although the long-term goal of nanotube researchers has been to replace digital CMOS devices made from silicon, and therefore to "extend Moore's law", a more realistic point of insertion into the market may be high-performance analogue radiofrequency (RF) devices, where manufacturing tolerances are relaxed and the performance metrics required for commercial systems are more suited to the materials and device properties of nanotubes. To realize this potential, it must be possible to economically manufacture dense aligned arrays of all-semiconducting nanotubes.

The use of massively parallel nanotube-based field-effect transistors (FETs) for applications such as mobile communication devices and radar is at present being investigated in both academic and industrial laboratories. So far, numerous nanotube-based FETs have been demonstrated using both single nanotubes and thin-film transistors made from mixtures of semiconducting and metallic nanotubes[5]. (The nanotubes in these devices can either be aligned or randomly oriented.) However, to achieve the highest performance, the nanotubes must be aligned at a high density (Fig. 1). Otherwise, the mobility is degraded from that of a pristine nanotube, and the fringe-field capacitance degrades the cut-off frequency by up to two orders of magnitude[6]. For this reason, the manufacturability of aligned arrays is very important, and several techniques have been investigated to solve the problems of nanotube alignment and purification: the two main techniques are 'grow in place' and 'deposition from solution'.

It has been proposed that nanotube-based FETs could, in principle, operate at frequencies well into the terahertz regime[6–11]. However, as it might not be possible to economically manufacture the perfectly dense perfectly aligned arrays containing only semiconducting nanotubes that are needed to achieve this level of performance, it is important to benchmark trade-offs that result from using less-than-perfect arrays. An intriguing aspect of nanotube-based FETs is a predicted inherent linearity[12], which is critically important for wireless communication systems. To confirm and quantify these and other device properties under realistic operating conditions, it is important to fabricate, test and demonstrate devices with high-density, aligned, all-semiconducting nanotubes in a scalable process, and to demonstrate such devices in actual working radio systems applications.

Here we review the progress so far in manufacturing, discuss the predicted and measured device properties as a function of manufacturing tolerances, and consider the implications for applications of single-walled nanotubes in analogue (as opposed to digital) RF devices and, ultimately, RF systems applications.

Grow in place by chemical vapour deposition

The most widely used method for growing single-walled nanotubes directly onto a substrate has been chemical vapour deposition (CVD). In general, a substrate holding metal catalyst particles is placed within a furnace with a flow of carbon feedstock gas and hydrogen gas at temperatures upwards of 900 °C. In such an environment, carbon nanotubes will grow from the catalyst particles with a diameter that is related to the size of these particles. To obtain aligned nanotubes during the CVD growth, multiple methods have been used to guide the alignment, such as applied electric fields[13,14], the gas flow[15–18] and interactions with the substrate. Of these, the most successful for obtaining highly dense perfectly aligned arrays of nanotubes has been surface-guided growth on single-crystal substrates such as sapphire or quartz[19–25]. Although the basic alignment mechanism remains unclear, it is assumed to involve the interactions between the nanotubes and the substrate's atomic steps, nanofacets or crystallographic lattice — or a mixture of these. Nanotube lengths of greater than 100 μm, linear densities of 10 nanotubes μm^{-1} (with peak values ~50 nanotubes μm^{-1}) and alignment within <0.01° have been achieved (Fig. 1c). Furthermore, procedures for transferring the aligned arrays to other substrates, such as SiO_2, or flexible substrates have been developed[26]. These techniques allow heterogeneous integration of aligned single-walled nanotubes with other materials that would not otherwise survive the high temperatures involved with the CVD nanotube growth process.

Nanotubes produced by the methane CVD method typically yield a mixture of two-thirds semiconducting nanotubes and one-third metallic nanotubes. The presence of the metallic nanotubes in parallel with the semiconducting nanotubes degrades device performance, especially the on/off ratio and the output resistance. Individual nanotube-based FETs have demonstrated on/off

Integrated Nanosystems Research Facility, Departmental of Electrical Engineering and Computer Science, University of California, Irvine, California 92697, USA.
*e-mail: pburke@uci.edu

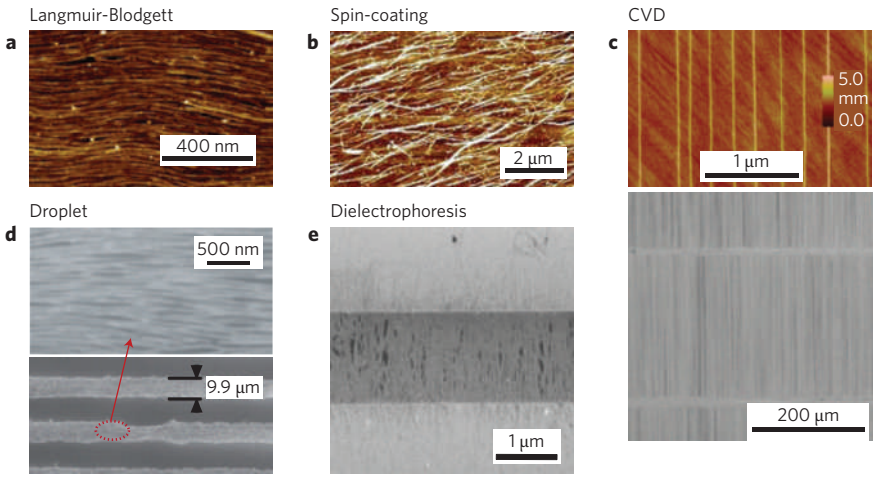

Figure 1 | Different ways to align nanotubes. To make high-frequency field-effect transistors from single-walled nanotubes (SWNTs), the nanotubes must be aligned, and they must also be long enough to span the source–drain channel. **a**, The Langmuir-Blodgett method can align SWNTs with a density of 30 nanotubes μm^{-1}, as shown in this atomic force microscopy image. Reproduced with permission from ref. 42 (© 2007 ACS). **b**, The spin-coating method is capable of aligning 10 nanotubes μm^{-2}, and an alignment of less than 10° of the radial axis, as shown in this atomic force microscopy image. Reproduced with permission from ref. 51 (© 2008 AAAS). **c**, Growing SWNTs by CVD on a single-crystal quartz substrate yields a high degree of alignment (<0.01°), as seen in the atomic force microscopy image (top). This method also produces nanotubes with lengths greater than 100 μm between the pair of catalyst lines, as shown in the scanning electron microscopy image (bottom). Reproduced with permission from ref. 29 (© 2009 ACS). **d**, The evaporating-droplet method produces densities of 10–20 nanotubes μm^{-1}, and alignment of less than 5°, as shown in these scanning electron microscopy images. Reproduced with permission from ref. 52 (© 2008 ACS). **e**, Dielectrophoresis uses the electric field to attract and align SWNTs between a pair of electrodes, as seen in this scanning electron microscopy image. Reproduced with permission from ref. 43 (© 2008 AIP).

ratios >10^6, but this ratio is much lower for combinations of metallic and semiconducting nanotubes. Although a degradation in the on/off ratio is acceptable for analogue RF applications (which relaxes the manufacturing requirements for analogue devices compared with those for digital devices), the presence of the metallic nanotubes also reduces the output resistance, which lowers the gain and frequency of operation, as discussed below. Therefore, it is necessary to devise strategies to selectively remove the metallic nanotubes while preserving (as much as possible) the semiconducting nanotubes.

Various gas-phase or plasma-etching methods have been developed to selectively remove metallic nanotubes[27,28]. Some of these methods can be incorporated into the growth process itself[29,30], and a combination of ethanol/methanol carbon feedstock mixture and copper nanoparticles as the catalyst was recently used to selectively grow >95% semiconducting nanotubes with a narrow diameter distribution and on/off ratios up to 85 (ref. 29). This selective growth is thought to be due to the OH^- radical from methanol selectively etching the metallic nanotubes during the growth owing to their smaller ionization potential compared with the semiconducting variety.

Using such preferential growth, one can further enhance the on/off current ratio by post-growth removal of the metallic nanotubes. One such method[27] involves the selective etching by hydrocarbonation of metallic nanotubes with diameters between ~1.3 and 1.6 nm using a 400 °C methane plasma treatment to achieve on/off ratios of 10^4–10^5. It is found that nanotubes having a diameter smaller than this range are indiscriminately etched regardless of being metallic or semiconducting, whereas those with larger diameters are not affected at all. This general processing method has the advantage that it is scalable and compatible with other traditional semiconductor processing techniques, although some semiconducting nanotubes are also damaged in the process.

'Wet etching' of metallic nanotubes has also been demonstrated. The process originates from the selective reaction of diazonium salts with the sidewalls of the nanotubes to significantly perturb their electronic and optical properties[31–33]. On/off current ratios are found to improve to 10^4.

The electrical breakdown method is a post-growth treatment that involves selectively 'burning off' metallic nanotubes by applying a strong gate-bias to deplete or turn off the semiconducting nanotube, thus forcing the current though the metallic nanotubes[34]. By ramping up the drain–source voltage, typically to greater than 30 V, it is possible to burn off the metallic nanotubes in the presence of oxygen. This process has been shown to improve the on/off current ratio upwards of 10^5, but this improvement comes at the cost of decreasing the pre-breakdown mobility owing to the inadvertent damaging of the semiconducting nanotubes as a result of

Table 1 | Ideal parameter values for making a high-frequency field-effect transistor from single-walled nanotubes.

Property/parameter	Target value or range	Justification
Diameter	1.5–2.0 nm	Current is largest in this range[54–55].
Chirality	Semiconducting and same (*n*,*m*)	To obtain identical transport properties.
Purity	>99% semiconducting nanotubes	No metallic nanotubes for high gain and high f_{max}.
Length	>1 μm	Nanotube length must be longer than the intended channel length.
Density	>10 nanotubes μm^{-1}	Reduces the parasitic capacitance per nanotube; increases current carrying capacity; improves impedance matching.
Alignment	All parallel	Results in higher transconductance and denser nanotube packing.
Uniformity	Wafer scale	Essential for large-scale processing.

the Joule heating produced by adjacent metallic nanotubes. Such reduction in mobility has been found to result in a post-breakdown mobility of up to half its pre-breakdown value for the standard two-thirds semiconductor/one-third metallic mix with densities of ~10 nanotubes μm^{-1} (refs 35–38). As the density is further increased and the distance between nanotubes becomes smaller, one would anticipate this collateral damage to adjacent nanotubes to be even more severe. From the scalability perspective, one would face the additional challenge of applying the necessary high voltage to each device on the wafer: an alternative approach that relies on microwaves[39] or light[40] to selectively burn off the metallic nanotubes has had some limited success.

Deposition from solution

Radiofrequency FETs can also be made using the 'deposition from solution' technique. A variety of techniques have been developed to sort as-produced single-walled nanotubes: these include selective chemistry, chromatographic separation and electrophoretic separation (see ref. 41 for a review). Using these techniques, or a combination of them, in the near future it should be feasible to prepare a solution of nanotubes in which all the nanotubes have the same length and the same chirality. (The chirality of a nanotube is denoted by two integers (n,m) which define the direction in which a hypothetical sheet of graphene would be rolled up to form that nanotube, and which also determine the diameter of the nanotube and whether it is metallic or semiconducting.)

When sorting nanotubes for applications in electronics the key challenges are: the economy of the process; the ability to sort large diameter (>1.5 nm) nanotubes; and the ability to sort sufficiently long nanotubes (ideally >1 μm) so that their length is longer than the source–drain spacing. Once these challenges (which do not seem to be insurmountable) have been solved, the remaining challenges will include learning how to deposit and assemble the nanotubes into an aligned array, and understanding how residual surfactants influence the electronic properties of the array once it has been assembled. (Nanotubes tend to be insoluble, so it is usually necessary to functionalize them first to make them soluble before they can be used in 'deposition from solution' methods.) Progress in these areas is reviewed below.

In the Langmuir-Blodgett technique a solution of nanotubes is spread on top of water in a Langmuir-Blodgett trough (in much the same way that oil spreads to form a slick on water), and movable barriers in the trough are used to subject the sample to cycles of compression and retraction, which results in the formation of a self-assembled monolayer of nanotubes. The nanotubes are then transferred onto a solid substrate by successively dipping the substrate through the monolayer. This method[42] has yielded linearly aligned tubes with packing densities of more than 30 nanotubes μm^{-1} (Fig. 1a), and the process is conceivably scalable to wafer-scale processing.

Nanotubes can be aligned using a.c. electric fields and then deposited between two closely spaced electrodes using dielectrophoresis[43–46] (Fig. 1e). A disadvantage of this process is its tendency to preferentially accumulate metallic nanotubes owing to their stronger polarizability compared with semiconducting nanotubes[47–50]. The other challenges include scaling up the process for wafer-scale production and combating the tendency of the nanotubes to form bundles during deposition.

Spin coating is a simple technique that involves spinning a wafer (usually made of silicon) at high speeds, and dripping a solution of nanotubes onto it so that they are deposited in a radially aligned pattern[51]. Although on/off ratios of $>10^5$ have been achieved, the devices have a low on-state current owing to the very large sheet resistance of the nanotube film. So far the densities obtained have been ~10 nanotubes μm^{-2} with moderate alignment (within ~10° of the radial axis[51]; Fig. 1b). (For randomly aligned nanotubes, researchers tend to quote areal rather than linear densities.)

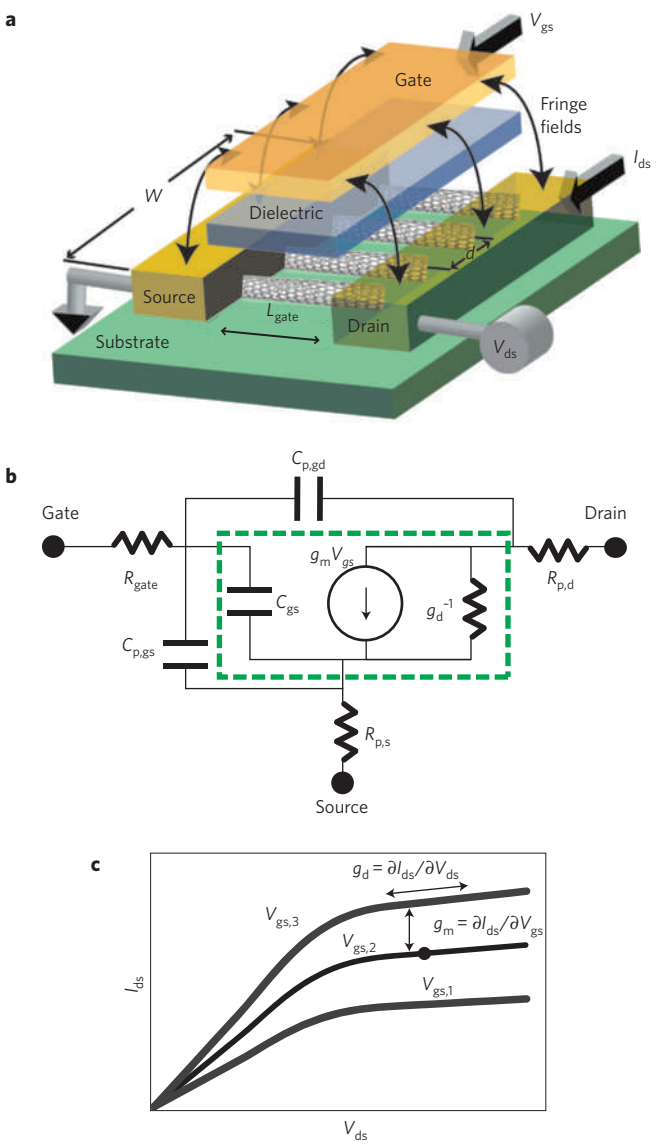

Figure 2 | The nanotube field-effect transistor. a, Schematic showing a FET in which the channel is an array of single-walled nanotubes: W is the gate width, L_{gate} is the gate length, d is the pitch (or spacing) of the nanotubes, V_{gs} and V_{ds} are the gate–source and drain–source voltages, and I_{ds} is the drain–source current. For RF-FETs, aligned arrays of nanotubes are needed to improve the impedance matching and increase the transconductance, the on-state current and the power density of the device. The fringe electrical fields from the gate to the source and drain give rise to the parasitic capacitance. **b**, A small-signal equivalent circuit for a nanotube-based FET where g_m is the transconductance, C_{gs} the intrinsic gate capacitance, and g_d the channel conductance (which can be significant if metallic nanotubes are present). These components encompass the 'intrinsic' portion of the device. The components outside the dashed line are parasitic elements: $C_{p,gs}$ and $C_{p,gd}$ are the gate–source and gate–drain parasitic capacitances, $R_{p,s}$ and $R_{p,d}$ are parasitic resistances for the source and drain, and R_{gate} is the resistance of the gate electrode. **c**, Schematic showing how the current through a nanotube transistor I_{ds} varies with the voltage across the transistor V_{ds} at three different values of the gate voltage V_{gs}. In practical applications the transistor is operated in the saturation regime at the values of V_{ds} and V_{gs} that give the optimum performance for a particular application (such as the highest gain or lowest noise). For d.c. voltages, the transconductance g_m depends on how I_{ds} changes with respect to the changes in V_{gs}, whereas the channel conductance g_d depends on how I_{ds} changes with respect to the changes in V_{ds}.

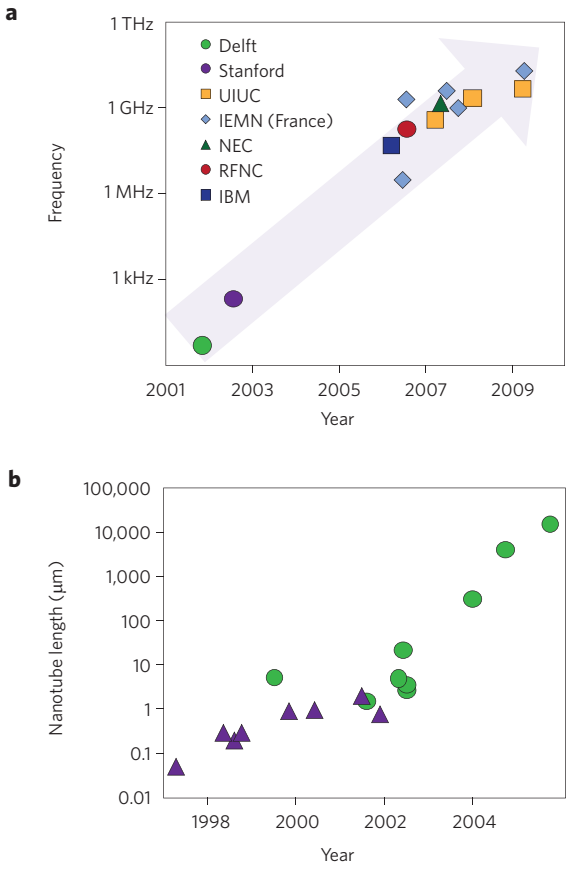

Figure 3 | Improvements over time. a, Maximum operating frequency (on a log scale) versus year for nanotube FETs. The maximum ring-oscillation frequency is plotted for the early work at Delft[69], Stanford[70] and IBM[71], and the cut-off frequency is plotted for the later work at RF Nano Corporation (RFNC)[60], NEC[72], Institut d'Electronique, de Microélectronique et de Nanotechnologie (IEMN)[68,73–75,77] and the University of Illinois at Urbana-Champaign (UIUC)[35,63,76]. **b**, Length of individual single-walled nanotubes (on a log scale) produced by laser ablation (purple triangles) and chemical vapour deposition (green circles) versus year. Although nanotubes longer than ~1 cm could conceivably be produced, the chambers of scanning electron microscopes are not large enough to characterize such long nanotubes. Ropes and yarns of much longer lengths have since been made. Figure reproduced with permission from ref. 78 (© 2007 World Scientific).

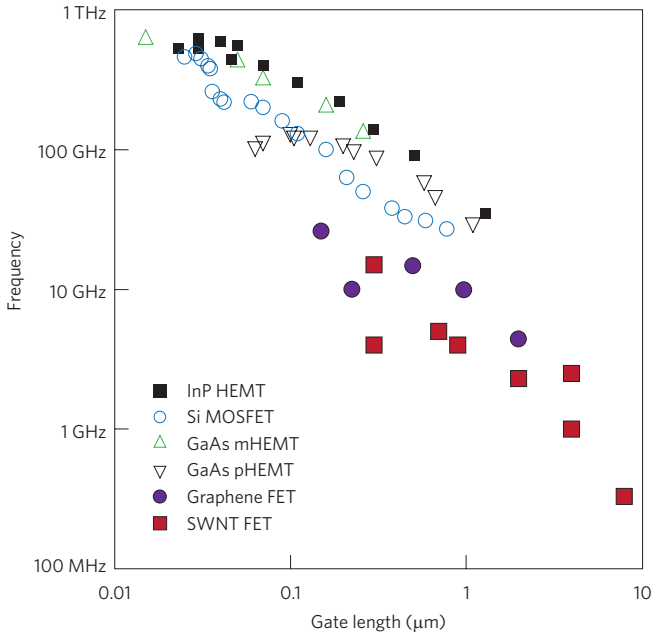

Figure 4 | Frequency performance of different materials. State-of-the-art frequency performance of traditional silicon[65,80–82] devices, III–V semiconductor devices (InP high electron mobility transistor (HEMT)[65], GaAs metamorphic-HEMT[65,83], and GaAs pseudomorphic-HEMT[65]), nanotube-based FETs[63,68,75,76] and graphene FETs[84–86,115] versus gate length. Data points for the nanotube-based FETs are the 'extrinsic' cut-off frequency. Silicon and III–V semiconductor data courtesy of Frank Schwierz.

The evaporating-droplet method has been successful in achieving self-assembled bands of high-density (~10–20 nanotubes μm^{-1}) aligned (within 5° of one another) nanotubes[52] (Fig. 1d). Similarly, using polar and nonpolar features patterned onto the substrate, linear droplet lines were formed and controlled nanotube deposition was achieved[53]. Although the process is conceivably scalable, the formation of periodic bands of aligned nanotubes could limit its utility for certain applications[52,53].

Table 1 summarizes the properties required of the final nanotube array for analogue RF electronics applications. Many of the techniques reviewed above can meet one or more of these metrics, such as diameters in the range 1.5–2 nm (required for high current[54,55]), but no single technique can meet all of them. Therefore, it is likely that some combination of the techniques will be required to meet the final requirements for practical device performance, which we discuss next.

Impact of array density on RF device performance

In the small-signal limit, the a.c. performance of RF transistors can be represented by a linear circuit model consisting of a voltage-dependent current source (the transconductance) plus associated resistances and capacitances (Fig. 2b). Such a model completely describes the input and output impedances, the voltage gain and the current gain, all of which depend on frequency.

Two different definitions of gain are widely used to characterize the frequency response of the transistor[56]: the current gain H_{21} is defined as the output current divided by the input current, and Mason's unilateral gain U is the power gain realized under conjugate impedance-matching at the input and output when the transistor is unilateralized (that is, embedded in a feedback network to isolate the output from the input) using a lossless reciprocal network[57]. For bipolar transistors in the low-frequency limit, H_{21} is better known as β, and can intuitively be considered as the current gain. For FET devices, the current gain is less intuitive, and the cut-off or transition frequency f_T — the frequency at which H_{21} falls to unity (0 dB) — is the most commonly quoted figure of merit, and is defined as such for both bipolar and FET technology. A more useful number for FETs is the maximum frequency of oscillation f_{max}, which is the frequency at which U drops to unity.

Using the effective RF circuit model shown in Fig. 2b, we can express the cut-off frequency of a nanotube FET as:

$$f_T = \frac{g_m}{2\pi} \frac{1}{(C_{gs} + C_{p,gs} + C_{p,gd})((R_{p,s} + R_{p,d})g_d + 1) + C_{p,gd}g_m(R_{p,s} + R_{p,d})} \quad (1)$$

where g_m is the transconductance, g_d is the drain conductance, C_{gs} is the gate capacitance, $C_{p,gd}$ and $C_{p,gs}$ are the parasitic gate-drain and gate-source capacitances, and $R_{p,s}$ and $R_{p,d}$ are the parasitic series resistance for the source and drain[58]. This is sometimes referred to as the extrinsic cut-off frequency to differentiate it from the intrinsic cut-off frequency (the calculated cut-off frequency when parasitics

are ignored). Sometimes, it is numerically justifiable to ignore the effects of parasitic circuit elements, but with nanotube-based FETs they are usually significant at all frequencies. Thus, the intrinsic cut-off frequency is given by:

$$f_{T,intrinsic} = \frac{g_m}{2\pi C_{gs}}$$

The intrinsic cut-off frequency can be considered the ultimate frequency performance of the device when it is not slowed down by external circuit elements. As $R_{p,s}$ and $R_{p,d}$ are usually external metal electrodes, they can often be made smaller with modest effort. The value of g_d would ideally be zero, but in the presence of metallic nanotubes, it can be significant. However, the most important extrinsic element is the parasitic capacitance. For an individual nanotube-based FET, the parasitic capacitance $C_{p,gs}$ is typically about two orders of magnitude larger than the intrinsic capacitance C_{gs}. (Typically, the values of both $C_{p,gs}$ and $C_{p,gd}$ are $\sim 10^{-16}$ F μm^{-1} of the gate width, whereas the C_{gs} of an individual nanotube is $\sim 10^{-17}$ F μm^{-1} of the nanotube length.) This reduces the cut-off frequency of individual nanotube-based FETs by about two orders of magnitude below its intrinsic limit[6,7,59–61].

To achieve the ultimate (intrinsic) limit, one must use very dense, parallel arrays of nanotubes because this increases g_m and C_{gs} while keeping the parasitic capacitance approximately constant. The need to use arrays to achieve the best possible performance is the most important conclusion of this Review Article.

To improve the frequency performance it is important to understand how the intrinsic cut-off frequency scales with gate length L_{gate}. First, as C_{gs} is proportional to the gate area, C_{gs} for a nanotube is proportional to L_{gate}. At present, it is not known how g_m for a nanotube scales with L_{gate}, so we use classical FET theory as a guide. If L_{gate} is long, the electric field E will be small (because $E = V_{ds}/L_{gate}$, where V_{ds} is the drain–source voltage), and the electron drift velocity will be given by $v_{drift} = \mu E$, where μ is the mobility. On the other hand, if L_{gate} is short, then E will be large, and v_{drift} will saturate at a value denoted by v_{sat}. Knowing v_{drift} we can calculate the transconductance and then the cut-off frequency in these two limits by using the following expression for the drain–source current $I_{ds} = v_{drift} ne$, where e is the charge of an individual electron, and the charge density $n = (C_{gs}/2eL_{gate})(V_{gs} - V_T)$, where V_{gs} is the gate–source voltage, and the threshold voltage V_T is related to the gate– and drain–source voltages by the expression $V_{ds} = (V_{gs} - V_T)$ in the current-saturation regime. For long gates and small electric fields we find the transconductance to be $\mu C_{gs}(V_{gs} - V_T)/L_{gate}^2$; for short gates and large electric fields it is given by $v_{sat}(C_{gs}/L_{gate})$. Consequently, the cut-off frequency can be represented by two limits:

$$f_{T,intrinsic} \approx \begin{cases} \mu(V_{gate} - V_T)/2\pi L_{gate}^2 & L_{gate\ large} \\ \dfrac{v_{sat}}{2\pi L_{gate}} & L_{gate\ small} \end{cases}$$

The question of the definition of 'large' versus 'small' depends on the details of the velocity-field curve for carbon nanotubes, which is difficult to measure. Still, it is generally accepted that GHz frequency operation will involve going into the short-gate-length regime, so the mobility will not be the appropriate figure of merit to determine the response time of the transistor. In nanotubes the value of v_{sat} is estimated to be ≈ 1.2–2×10^7 cm s^{-1} (based on carefully modelling both the d.c.[62] and RF[63] performance). Using these values, the predicted 'intrinsic' cut-off frequency will be $\approx$ 20–30 GHz/L_{gate} (μm) (depending on the value of v_{sat} assumed), which is comparable to the best III–V semiconductors.

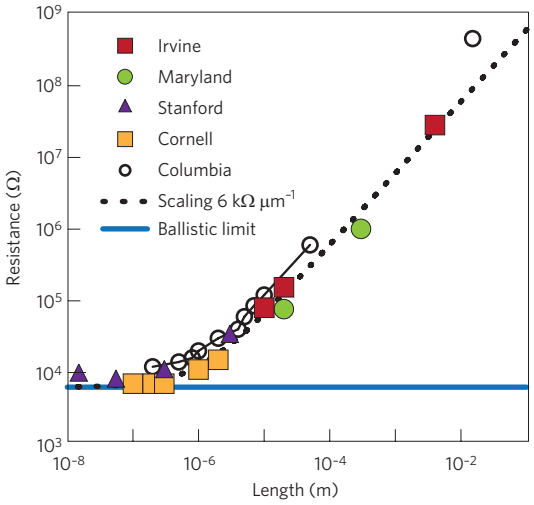

Figure 5 | Resistance performance. Resistance versus length for individual single-walled nanotubes at room temperature (except for the data point at 76 kΩ, 20 μm (left-most green circle), which was measured at 4.2 K; ref. 62) from various labs around the world. The Cornell University data[90] were taken by using an atomic force microscope to measure the voltage drop on an individual nanotube, whereas the Columbia University data[91,92] were taken with multiple contacts on an individual nanotube. The data points from University of California, Irvine[88,89], University of Maryland, College Park[4,62] and Stanford University[93–95] are for distinct nanotubes. All the data are consistent with single-walled nanotubes having a resistance of about 6 kΩ μm^{-1} (dotted line). The ballistic limit (solid blue line) is the lowest contact resistance allowed by quantum mechanics. Reproduced with permission from ref. 87 (© 2009 Wiley).

On the other hand, for long-channel devices (such as printed electronic devices with channel lengths that are longer than 10 μm), the effective mobility determines the cut-off frequency, and here individual nanotubes also have mobilities comparable to the best III–V semiconductors. So far, nanotube-array devices that realize this intrinsic limit have not yet been demonstrated, owing to limitations from parasitic capacitances (see below), but with dense enough arrays, it should be possible to approach this intrinsic speed limit.

In the extreme short-channel limit (where transport is ballistic from source to drain), it has been argued that the carrier-injection velocity into the channel strongly influences the cut-off frequency, so the mobility also becomes important in this limit[64]. Moreover, we should note that the above arguments apply mainly to 'ideal' structures where short-channel effects, parasitic effects and the overall design (for example, metal oxide field-effect transistor (MOSFET) versus high electron mobility transistor (HEMT)) are not important, so they provide only a qualitative guide in the extreme short-channel limit. (See ref. 65 for more details).

How does one construct a thin-film transistor (TFT) that achieves the intrinsic limit discussed above? In general, the best approach is to reduce the relative importance of the parasitic capacitances (which are mainly due to the fringe fields from the electrodes, and depend only mildly on the device geometry). Thus, by increasing the number of nanotubes per width, one increases the transconductance g_m without a significant increase in the parasitic capacitance, allowing the ultimate limit to be reached. In this context, it is important to quantify the relationship between the cut-off frequency and the intrinsic cut-off frequency as a function of nanotube array density.

In the limit of sparse nanotube arrays (that is, when the pitch (or spacing) between the nanotubes d is larger than gate–tube

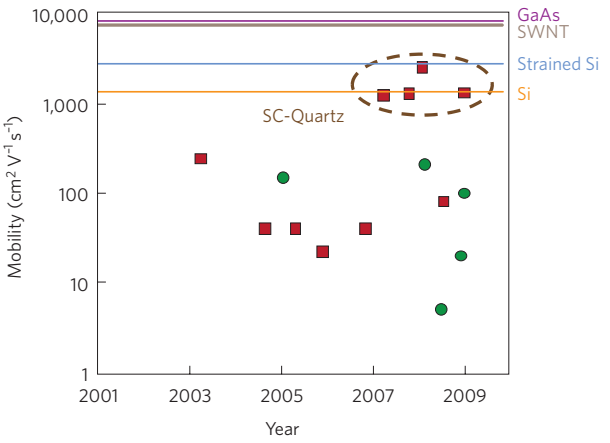

Figure 6 | Mobility performance. For long-channel devices, the mobility is important in achieving a large transconductance and a high cut-off frequency. This plot shows mobility versus year for TFTs made by two methods: devices made from single-walled nanotubes grown by CVD are shown as red squares[35,76,96-103], and devices made from nanotubes deposited from solution are shown as green circles (refs 51,52,104,105 and M. Ishida, S. Toguchi, H. Hongo and F. Nihet, unpublished observation). TFTs grown by CVD on single-crystal quartz substrates (red squares inside dashed line) have the highest mobilities. As a comparison, mobility values for n-type (undoped) silicon, strained silicon, an individual single-walled nanotube (diameter ~2 nm) and gallium arsenide are also shown.

separation), and neglecting $R_{p,s}$ and $R_{p,d}$ in equation (1), the cut-off frequency[7] in the presence of parasitic capacitances can be written as:

$$f_T = f_{T,\text{intrinsic}} \left(\frac{1}{1 + \frac{C_w}{C_{gs,1}} d} \right) \quad (2)$$

where $C_{gs,1}$ is the nanotube–gate capacitance of an individual nanotube, and C_w is the parasitic capacitance per gate width defined as $(C_{p,gd} + C_{p,gs})/W$, where W is the gate width (see Fig. 2). Typically[6], C_w is ~10^{-16} F μm^{-1} and $C_{gs,1} \approx 10^{-17}$ F × L_{gate} (μm) so that, ideally, one wants the spacing between the nanotubes to be less than 0.1 μm (that is, a density of 10 nanotubes μm^{-1} or higher), for the cut-off frequency not to be significantly degraded by the external (parasitic) capacitance. This is achievable using some of the deposition methods described above.

Although the nanotube density is the critical parameter, g_d, $R_{p,s}$, and $R_{p,d}$ can cause further degradation in f_T as seen in equation (1). At even higher densities, screening by adjacent nanotubes will effect the values (per nanotube) of the transconductance and gate capacitance[35,66]. However, these effects cancel in the calculation of the cut-off frequency, so equation (2) is still valid in the presence of screening, but the value of $C_{gs,1}$ will be reduced compared with the sparse case.

For RF applications, power gain is the important figure of merit (rather than current gain), so f_{max} is also an important parameter. A typical approximation for f_{max} is (see ref. 58):

$$f_{max} \approx \frac{f_T}{2(g_d(R_{p,s} + R_{gate}) + 2\pi f_T C_{p,gd} R_{gate})^{\frac{1}{2}}}$$

where R_{gate} is the gate resistance. The value of f_{max} can be made as high as possible by increasing the density of the nanotubes in the array to make $C_{p,gd}$ as small as possible. However, the presence of metallic nanotubes in the array will lead to a non-zero value of g_d, which will reduce f_{max}, and this is one of the reasons for removing the metallic nanotubes. A comprehensive study of the effects of both R_{gate} and the presence of metallic nanotubes on f_{max} is an important next step in the development of RF devices[67].

Although f_T and f_{max} are generally of the same order of magnitude, either one can be higher than the other depending on the device characteristics (see, for example, Fig. 14 in ref. 65). This is especially important for nanotube transistors, where f_T can be an order of magnitude higher than f_{max} (ref. 68). Thus, both f_T and f_{max} should be compared when comparing the performance of different nanotube transistors.

Devices and measurements

Frequency performance has improved in the past few years, with individual nanotube-based FETs reaching frequencies up to 52 MHz in a multistage ring-oscillator[69–71], and arrays of nanotubes showing cut-off frequencies of up to ~10 GHz (refs 35,60,63,68,72–77; see Fig. 3a). The maximum length of nanotubes has also increased[78] (Fig. 3b). The next challenge on the road to higher frequencies is to increase the nanotube density and the percentage of semiconducting nanotubes.

The highest frequencies reported so far have been for nanotube devices made from samples with about two-thirds semiconducting nanotubes and densities of 5 nanotubes μm^{-1} grown by CVD on quartz[63,76], or from samples that are mostly (90–95%) metallic but have been deposited at higher densities with dielectrophoresis[68,75]. Both device families achieve cut-off frequencies of ~10 GHz with gate lengths ~0.3 μm, indicating that if the fraction of semiconducting nanotubes or density can be improved, the cut-off frequency can be substantially increased. This should be possible by starting with the samples of purified semiconducting nanotubes that have recently become available in a number of labs (see, for example, refs 68 and 79).

To compare nanotubes with other materials, we plot the cut-off frequency versus gate length for nanotubes, graphene and various semiconductors in Fig. 4 (see refs 63,65,68,75,76,80–86). Although it is often assumed that high-mobility materials are needed to make high-speed FETs, this relationship generally only holds true for devices with long channels, as discussed above. For example, for submicrometre gate lengths, the speed advantages of III–V semiconductors such as GaAs and InP over Si-MOSFETs[65] are mainly due to higher saturation velocities. Graphene-based FETs use two-dimensional sheets of carbon atoms as the channel material (as opposed to the one-dimensional tubes of carbon atoms used in nanotube-based FETs), and a recent report of an extrinsic cut-off frequency of ~26 GHz for a 150-nm-gate-length device is on a par with the performance of the best nanotube-based FETs if we allow for the difference in gate length[85] (Fig. 4). However, as described above, the use of denser arrays will lead to increases in the cut-off frequency for nanotube FETs.

In contrast to submicrometre devices, the effective mobility is an important figure-of-merit for TFT devices with long channel lengths. It is generally agreed[3] that electron–phonon scattering limits the peak mobility of an individual nanotube to between 6,000 and 10,000 cm^2 V^{-1} s^{-1}, with the resistance being about 6 kΩ μm^{-1} (Fig. 5 and refs 87–95). The mean free-path inferred from these measurements (at low electric fields) is ~1 μm. For arrays or thin films of nanotubes, the effective mobility is related to the nanotube density, alignment and fraction of semiconducting nanotubes[5]. It is generally believed that a thin film of nanotubes, suitably prepared, should be able to achieve an 'effective' mobility comparable to that of a single nanotube level, but this has not been demonstrated yet.

In Fig. 6, we plot the mobility versus year for nanotube films prepared by the two methods discussed earlier — grow in place with CVD, and deposition from solution — along with the mobility of

a pristine nanotube and the mobilities reported for other materials (refs 35,51,52,76,96–105 and M. Ishida, S. Toguchi, H. Hongo and F. Nihet, unpublished observation). We plot mobility values computed using $\mu = (l/WC_{gs})(1/V_{ds})\partial I_{ds}/\partial V_{gs}$ from data measured typically in the linear regime (low V_{ds}). However, devices typically operate in the saturation regime (high V_{ds}), so the mobility numbers quoted in the literature (typically measured at low V_{ds}) are not always a good guide to device performance.

The mobilities of randomly aligned mats of nanotubes grown in place on silicon and those deposited from solution are comparable, with wide scatter due to differences in the nanotube density, average length and, possibly, other parameters. It is generally found that the mobility (which should be independent of gate length for single nanotubes) increases with increasing gate length, even for nanotube films of nominally the same quality. Generally speaking, we still do not have a reliable method for predicting the final device mobility based on the detailed preparation parameters. However, the mobility of nanotube arrays grown by CVD on quartz[35,76,101,102] are much higher than those deposited from solution onto other substrates.

Nanotubes deposited from solution have much higher mobilities than organic semiconductors (which typically have mobilities of ~1 $cm^2\ V^{-1}\ s^{-1}$; ref. 106), and therefore they could compete with organics in applications that require only moderate mobilities such as low-cost printed electronic circuits. Although techniques for making printed circuits typically achieve resolutions (and hence gate lengths) of ~10 μm, the recent introduction of self-aligned techniques to the manufacture of printed circuits has allowed submicrometre gate lengths to be achieved, even in inkjet printed devices[107]. This approach has been shown to minimize the overlap parasitic capacitance and has made it possible to achieve a cut-off frequency 1.6 MHz from a starting material with a mobility of ~0.2 $cm^2\ V^{-1}\ s^{-1}$ and a gate length of 200 nm. If this new self-aligned approach to making printed electronics could be combined with the nanotube TFTs made with the solution-based approach (which have mobilities up to about 200 $cm^2\ V^{-1}\ s^{-1}$; M. Ishida, S. Toguchi, H. Hongo and F. Nihet, unpublished observation), it might be possible (neglecting velocity saturation effects discussed above) to increase the cut-off frequency by a factor of 1,000 to give $f_T > 1$ GHz. Such an accomplishment would represent a great leap forward on the road to high-frequency low-cost circuit applications such as all-printed RF identification tags[108].

Demonstrations of nanotubes in RF applications

Recently, several groups have gone beyond device characterization and demonstrated applications in actual radio systems. Although these radios are not yet commercially competitive with existing systems, it is an important milestone to be able to demonstrate operating systems.

Our lab at the University of California, Irivne[109] and another lab at the University of California, Berkeley[110] have used a nanotube as the demodulator in a radio receiver, and have demonstrated a functioning radio that can pick up a signal generated in the lab by a separate generator and play music broadcast wirelessly across a room. Since the demodulation occurs owing to the nonlinearity in the source–drain current–voltage characteristics, it does not matter whether a metallic or semiconducting nanotube is used in this case. The nanotube itself simply detected an amplitude-modulated (AM) signal (replacing the diode in a classical AM radio) and, as such, does not present any particular advantage, other than small size. Moreover, the overall radio system is still large because the external components (the antenna, battery, audio amplifier and so on) are still large (Fig. 7). The UC Berkeley work adds further functionality by using the mechanical resonance frequency of the nanotube as an integrated RF filter, an elegant step towards an integrated nanoradio, but at the cost of requiring a high vacuum. Furthermore, neither of these radios were sensitive

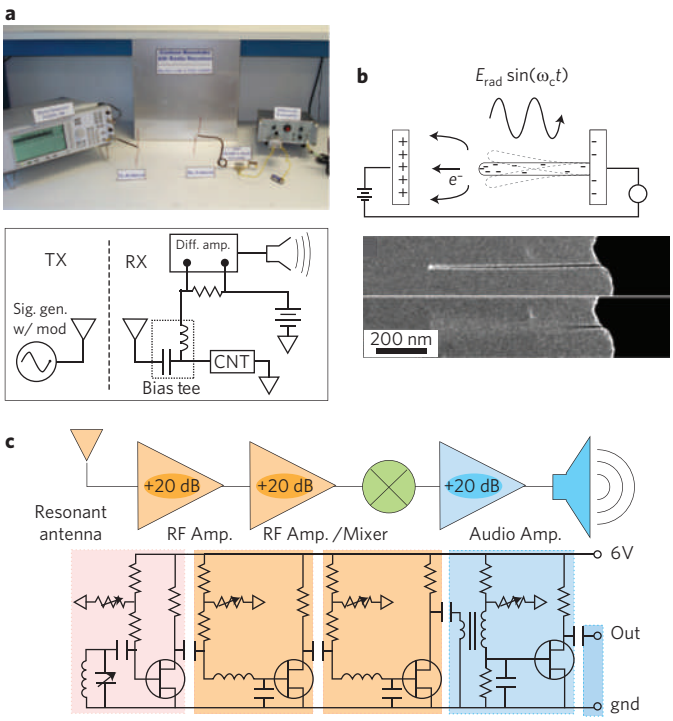

Figure 7 | Nanotubes are performing increasingly complex roles in AM radios. a, A nanotube (CNT) acts as a RF detector in an AM radio. The other components in this demonstration include a signal generator, which is used to transmit (TX) wirelessly an amplitude-modulated signal (sig. gen. w/mod) to the receiver (RX), which consists of a bias tee, a differential amplifier (diff. amp.), a speaker and battery. Reproduced with permission from ref. 109 (© 2007 ACS). **b**, A nanotube in high vacuum acts as a RF detector and an integrated RF filter in an AM radio, where an oscillating electric field ($E_{rad}\sin(\omega_c t)$) induces the vibration of the tube. Reproduced with permission from ref. 110 (© 2007 ACS). **c**, Nanotube-based FETs act as the RF pre-amplifier, detector (mixer) and audio-frequency amplifier, thus demonstrating a complete AM radio system. Reproduced with permission from ref. 76 (© 2008 PNAS).

enough to receive weak radio signals from local radio stations due to lack of an RF pre-amplifier at the front end.

A recent collaboration between the University of Illinois at Urbana-Champaign and Northrop Grumman has demonstrated the first RF amplifier based on a nanotube FET, and used it in an entire AM radio system[76]. Separate nanotube transistors also functioned as the RF detector (actually mixer) and audio amplifier. Because an RF pre-amplifier was used, the radio was able to receive weak signals from a local radio station. This demonstrates the application of nanotube electronics into a fully functional system.

Although these demonstrations show that it is possible to make nanoscale components, a true nanoradio would require all the components — including the power source (battery), antenna and the signal-processing elements — to be nanoscale. Using the RF field itself as a power source would completely obviate the need for the battery, while the use of on-chip antennas[111] or even nano-antennas[112,113] would allow for much smaller radios. More research is needed to address the trade-offs between efficiency, required external power, antenna size and heating. Based on standard CMOS technology, we have argued that a single-chip radio system (including antenna and providing space for on-board sensors) of size 100 × 100 × 1 μm is feasible, which begins to approach the size of a single living cell[114]. A true nanoradio should eventually be possible with further developments in nanotechnology.

Summary

To obtain high-performance nanotube-based RF-FETs, dense aligned arrays of all-semiconducting nanotubes are required. Progress in this direction has been rapid, and there are several potential routes towards manufacturing such materials. The advantages of high linearity predicted for one-dimensional materials, together with relaxed manufacturing tolerances, may be the defining advantage over other materials for analogue RF devices. Initial systems have been demonstrated by multiple research labs, and if the previous rate of progress is any indication, it is entirely feasible that, rather than extending Moore's law for digital electronics, the initial point of insertion of nanotube technology into commercial electronics markets will be in wireless communications systems of various kinds.

References

1. Dresselhaus, M. S., Dresselhaus, G. & Eklund, P. C. *Science of Fullerenes and Carbon Nanotubes*. (Academic Press, 1996).
2. Saito, R., Dresselhaus, G. & Dresselhaus, M. S. *Physical Properties of Carbon Nanotubes*. (Imperial College Press, 1998).
3. Zhou, X. J., Park, J. Y., Huang, S. M., Liu, J. & McEuen, P. L. Band structure, phonon scattering, and the performance limit of single-walled carbon nanotube transistors. *Phys. Rev. Lett.* **95,** 146805 (2005).
4. Durkop, T., Getty, S. A., Cobas, E. & Fuhrer, M. S. Extraordinary mobility in semiconducting carbon nanotubes. *Nano Lett.* **4,** 35–39 (2004).
5. Cao, Q. & Rogers, J. Ultrathin films of single-walled carbon nanotubes for electronics and sensors: A review of fundamental and applied aspects. *Adv. Mater.* **21,** 29–53 (2009).
6. Burke, P. J. AC performance of nanoelectronics: Towards a ballistic THz nanotube transistor. *Solid State Electron.* **40,** 1981–1986 (2004).
7. Guo, J., Hasan, S., Javey, A., Bosman, G. & Lundstrom, M. Assessment of high-frequency performance potential of carbon nanotube transistors. *IEEE Trans. Nanotech.* **4,** 715–721 (2005).
8. Alam, K. & Lake, R. Performance of 2 nm gate length carbon nanotube field-effect transistors with source/drain underlaps. *Appl. Phys. Lett.* **87,** 073104 (2005).
9. Hasan, S., Salahuddin, S., Vaidyanathan, M. & Alam, A. A. High-frequency performance projections for ballistic carbon-nanotube transistors. *IEEE Trans. Nanotech.* **5,** 14–22 (2006).
10. Castro, L. C. *et al.* Method for predicting f_T for carbon nanotube FETs. *IEEE Trans. Nanotech.* **4,** 699–704 (2005).
11. Yoon, Y., Ouyang, Y. & Guo, J. Effect of phonon scattering on intrinsic delay and cutoff frequency of carbon nanotube FETs. *IEEE Trans. Electron Dev.* **53,** 2467–2470 (2006).
12. Baumgardner, J. E. *et al.* Inherent linearity in carbon nanotube field-effect transistors. *Appl. Phys. Lett.* **91,** 052107 (2007).
13. Ural, A., Li, Y. M. & Dai, H. J. Electric-field-aligned growth of single-walled carbon nanotubes on surfaces. *Appl. Phys. Lett.* **81,** 3464–3466 (2002).
14. Joselevich, E. & Lieber, C. M. Vectorial growth of metallic and semiconducting single-wall carbon nanotubes. *Nano Lett.* **2,** 1137–1141 (2002).
15. Huang, S. M., Cai, X. Y. & Liu, J. Growth of millimeter-long and horizontally aligned single-walled carbon nanotubes on flat substrates. *J. Am. Chem. Soc.* **125,** 5636–5637 (2003).
16. Huang, S., Woodson, M., Smalley, R. & Liu, J. Growth mechanism of oriented long single walled carbon nanotubes using fast-heating chemical vapor deposition process. *Nano Lett.* **4,** 1025–1028 (2004).
17. Yu, Z., Li, S. & Burke, P. J. Synthesis of aligned arrays of millimeter long, straight single walled carbon nanotubes. *Chem. Mater.* **16,** 3414–3416 (2004).
18. Huang, L. *et al.* Cobalt ultrathin film catalyzed ethanol chemical vapor deposition of single-walled carbon nanotubes. *J. Phys. Chem. B* **110,** 11103–11109 (2006).
19. Ismach, A., Segev, L., Wachtel, E. & Joselevich, E. Atomic-step-templated formation of single wall carbon nanotube patterns. *Angew. Chem. Int. Ed.* **43,** 6140–6143 (2004).
20. Ago, H. *et al.* Aligned growth of isolated single-walled carbon nanotubes programmed by atomic arrangement of substrate surface. *Chem. Phys. Lett.* **408,** 433–438 (2005).
21. Han, S., Liu, X. L. & Zhou, C. W. Template-free directional growth of single-walled carbon nanotubes on a- and r-plane sapphire. *J. Am. Chem. Soc.* **127,** 5294–5295 (2005).
22. Kocabas, C. *et al.* Guided growth of large-scale, horizontally aligned arrays of single-walled carbon nanotubes and their use in thin-film transistors. *Small* **1,** 1110–1116 (2005).
23. Ago, H. *et al.* Competition and cooperation between lattice-oriented growth and step-templated growth of aligned carbon nanotubes on sapphire. *Appl. Phys. Lett.* **90,** 123112 (2007).
24. Ding, L., Yuan, D. N. & Liu, J. Growth of high-density parallel arrays of long single-walled carbon nanotubes on quartz substrates. *J. Am. Chem. Soc.* **130,** 5428–5429 (2008).
25. Zhou, W. W., Rutherglen, C. & Burke, P. Wafer scale synthesis of dense aligned arrays of single-walled carbon nanotubes. *Nano Research* **1,** 158–165 (2008).
26. Kang, S. J. *et al.* Printed multilayer superstructures of aligned single-walled carbon nanotubes for electronic, applications. *Nano Lett.* **7,** 3343–3348 (2007).
27. Zhang, G. *et al.* Selective etching of metallic carbon nanotubes by gas-phase reaction. *Science* **314,** 974–977 (2006).
28. Yang, C. M. *et al.* Preferential etching of metallic single-walled carbon nanotubes with small diameter by fluorine gas. *Phys. Rev. B.* **73,** 075419 (2006).
29. Ding, L. *et al.* Selective growth of well-aligned semiconducting single-walled carbon nanotubes. *Nano Lett.* **9,** 800–805 (2009).
30. Li, Y. *et al.* Preferential growth of semiconducting single-walled carbon nanotubes by a plasma enhanced CVD method. *Nano Lett.* **4,** 317–321 (2004).
31. An, L., Fu, Q., Lu, C. & Liu, J. A simple chemical route to selectively eliminate metallic carbon nanotubes in nanotube network devices. *J. Am. Chem. Soc.* **126,** 10520–10521 (2004).
32. Balasubramanian, K., Sordan, R., Burghard, M. & Kern, K. A selective electrochemical approach to carbon nanotube field-effect transistors. *Nano Lett.* **4,** 827–830 (2004).
33. Strano, M. S. *et al.* Electronic structure control of single-walled carbon nanotube functionalization. *Science* **301,** 1519–1522 (2003).
34. Collins, P. C., Arnold, M. S. & Avouris, P. Engineering carbon nanotubes and nanotube circuits using electrical breakdown. *Science* **292,** 706–709 (2001).
35. Kang, S. J. *et al.* High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes. *Nature Nanotech.* **2,** 230–236 (2007).
36. Amlani, I. *et al.* in *8th IEEE Conf. Nanotech* 239–242 (IEEE, 2008).
37. Lin, A. *et al.* Threshold voltage and on-off ratio tuning for multiple-tube carbon nanotube FETs. *IEEE Trans. Nanotech.* **8,** 4–9 (2009).
38. Ryu, K. *et al.* CMOS-analogous wafer-scale nanotube-on-insulator approach for submicrometer devices and integrated circuits using aligned nanotubes. *Nano Lett.* **9,** 189–197 (2009).
39. Shim, H., Song, J., Kwak, Y., Kim, S. & Han, C. Preferential elimination of metallic single-walled carbon nanotubes using microwave irradiation. *Nanotechnology* **20,** 065707 (2009).
40. Huang, H., Maruyama, R., Noda, K., Kajiura, H. & Kadono, K. Preferential destruction of metallic single-walled carbon nanotubes by laser irradiation. *J. Phys. Chem. B* **110,** 7316–7320 (2006).
41. Hersam, M. Progress towards monodisperse single-walled carbon nanotubes. *Nature Nanotech.* **3,** 387–394 (2008).
42. Li, X. *et al.* Langmuir-Blodgett assembly of densely aligned single-walled carbon nanotubes from bulk materials. *J. Am. Chem. Soc.* **129,** 4890–4891 (2007).
43. Rutherglen, C., Jain, D. & Burke, P. RF resistance and inductance of massively parallel single walled carbon nanotubes: Direct, broadband measurements and near perfect 50 ohm impedance matching. *Appl. Phys. Lett.* **93,** 083119 (2008).
44. Krupke, R., Linden, S., Rapp, M. & Hennrich, F. Thin films of metallic carbon nanotubes prepared by dielectrophoresis. *Adv. Mater.* **18,** 1468–1468 (2006).
45. Boccaccini, A. R. *et al.* Electrophoretic deposition of carbon nanotubes. *Carbon* **44,** 3149–3160 (2006).
46. Morgan, H. & Green, N. G. *AC Electrokinetics: Colloids and Nanoparticles* (Research Studies Press, 2003).
47. Krupke, R., Hennrich, F., Lohneysen, H. & Kappes, M. M. Separation of metallic from semiconducting single-walled carbon nanotubes. *Science* **301,** 344–347 (2003).
48. Krupke, R., Hennrich, F., Kappes, M. & Lohneysen, H. Surface conductance induced dielectrophoresis of semiconducting single-walled carbon nanotubes. *Nano Lett.* **4,** 1395–1400 (2004).
49. Baik, S., Usrey, M., Rotkina, L. & Strano, M. Using the selective functionalization of metallic single-walled carbon nanotubes to control dielectrophoretic mobility. *J. Phys. Chem. B* **108,** 15560–15564 (2004).
50. Kim, Y. *et al.* Dielectrophoresis of surface conductance modulated single-walled carbon nanotubes using catanionic surfactants. *J. Phys. Chem. B* **110,** 1541–1545 (2006).
51. LeMieux, M. C. *et al.* Self-sorted, aligned nanotube networks for thin-film transistors. *Science* **321,** 101–104 (2008).
52. Engel, M. *et al.* Thin film nanotube transistors based on self-assembled, aligned, semiconducting carbon nanotube arrays. *ACS Nano* **2,** 2445–2452 (2008).
53. Sharma, R., Lee, C. Y., Choi, J. H., Chen, K. & Strano, M. S. Nanometer positioning, parallel alignment, and placement of single anisotropic nanoparticles using hydrodynamic forces in cylindrical droplets. *Nano Lett.* **7,** 2693–2700 (2007).
54. Chen, Z., Appenzeller, J., Knoch, J., Lin, Y.-M. & Avouris, P. The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors. *Nano Lett.* **5,** 1497–1502 (2005).

55. Kim, W. *et al.* Electrical contacts to carbon nanotubes down to 1 nm in diameter. *Appl. Phys. Lett.* **87,** 173101 (2005).
56. Liu, W. Fundamentals of III-V devices: HBTs, MESFETs, and HFETs/HEMTs. (Wiley, 1999).
57. Gupta, M. S. Power gain in feedback amplifiers, a classic revisited. *IEEE Trans. Microw. Theory* **40,** 864–879 (1992).
58. Schwierz, F. & Liou, J. J. *Modern Microwave Transistors: Theory, Design, and Performance*. (Wiley-Interscience, 2003).
59. Akinwande, D., Close, G. E. & Wong, H. S. P. Analysis of the frequency response of carbon nanotube transistors. *IEEE Trans. Nanotech.* **5,** 599–605 (2006).
60. Wang, D., Yu, Z., McKernan, S. & Burke, P. Ultra high frequency carbon nanotube transistor based on a single nanotube. *IEEE Trans. Nanotech.* **6,** 400–403 (2007).
61. Chaste, J. *et al.* Single carbon nanotube transistor at GHz frequency. *Nano Lett.* **8,** 525–528 (2008).
62. Chen, Y. F. & Fuhrer, M. S. Electric field-dependent charge-carrier velocity in semiconducting carbon nanotubes. *Phys. Rev. Lett.* **95,** 236803 (2005).
63. Kocabas, C. *et al.* High-frequency performance of submicrometer transistors that use aligned arrays of single-walled carbon nanotubes. *Nano Lett.* **8,** 1937–1943 (2009).
64. Lundstrom, M. Elementary scattering theory of the Si MOSFET. *IEEE Electr. Device Lett.* **18,** 361–363 (1997).
65. Schwierz, F. & Liou, J. J. RF transistors: Recent developments and roadmap toward terahertz applications. *Solid State Electron.* **51,** 1079–1091 (2007).
66. Cao, Q. *et al.* Gate capacitance coupling of singled-walled carbon nanotube thin-film transistors. *Appl. Phys. Lett.* **90,** 023516 (2007).
67. Castro, L. C. & Pulfrey, D. L. Extrapolated f_{max} for carbon nanotube field-effect transistors. *Nanotechnology* **17,** 300–304 (2006).
68. Nougaret, L. *et al.* 80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes. *Appl. Phys. Lett.* **94,** 243505 (2009).
69. Bachtold, A., Hadley, P., Nakanishi, T. & Dekker, C. Logic circuits with carbon nanotube transistors. *Science* **294,** 1317–1320 (2001).
70. Javey, A., Wang, Q., Ural, A., Li, Y. M. & Dai, H. J. Carbon nanotube transistor arrays for multistage complementary logic and ring oscillators. *Nano Lett.* **2,** 929–932 (2002).
71. Chen, Z. H. *et al.* An integrated logic circuit assembled on a single carbon nanotube. *Science* **311,** 1735–1735 (2006).
72. Narita, K., Hongo, H., Ishida, M. & Nihey, F. High-frequency performance of multiple-channel carbon nanotube transistors. *Phys. Status Solidi A* **204,** 1808–1813 (2007).
73. Bethoux, J. M. *et al.* Active properties of carbon nanotube field-effect transistors deduced from S parameters measurements. *IEEE Trans. Nanotech.* **5,** 336–342 (2006).
74. Bethoux, J. M. *et al.* An 8-GHz f_T carbon nanotube field-effect transistor for gigahertz range applications. *IEEE Electron Dev. Lett.* **27,** 681–683 (2006).
75. Louarn, A. L. *et al.* Intrinsic current gain cutoff frequency of 30 GHz with carbon nanotube transistors. *Appl. Phys. Lett.* **90,** 233108 (2007).
76. Kocabas, C. *et al.* Radio frequency analog electronics based on carbon nanotube transistors. *Proc. Natl Acad. Sci. USA* **105,** 1405–1409 (2008).
77. Chimot, N. *et al.* Gigahertz frequency flexible carbon nanotube transistors. *Appl. Phys. Lett.* **91,** 153111 (2007).
78. Burke, P. J. *Nanotubes and Nanowires* (World Scientific, 2007).
79. Rutherglen, C. *Carbon Nanotube Based Analog RF Devices* PhD thesis, Univ. California, Irvine (2009).
80. Dimitrov, V. *et al.* Small-signal performance and modeling of sub-50 nm nMOSFETs with f_T above 460 GHz. *Solid State Electron.* **52,** 899–908 (2008).
81. Stork, J. in *Proc. Symp. VLSI Tech. Dig.* 1–2 (IEEE, 2006).
82. Lee, S. *et al.* in *Electron Devices Meeting IEDM* 255–258 (IEEE, 2007).
83. Yeon, S., Park, M., Choi, J. & Seo, K. in *Electron Devices Meeting IEDM* 613–616 (IEEE, 2007).
84. Moon, J. S. *et al.* Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates. *IEEE Electr. Device Lett.* **30,** 650–652 (2009).
85. Lin, Y. *et al.* Operation of graphene transistor at gigahertz frequencies. *Nano Lett.* **9,** 422–426 (2009).
86. Meric, I., Baklitskaya, P., Kim, P. & Shepard, K. RF performance of top-gated, zero-bandgap graphene field-effect transistor. *Electron Devices Meeting IEDM* 1–4 (IEEE, 2008).
87. Rutherglen, C. & Burke, P. Nanoelectromagnetics: Circuit and electromagnetic properties of carbon nanotubes. *Small* **5,** 884–906 (2009).
88. Li, S., Yu, Z., Yen, S. F., Tang, W. C. & Burke, P. J. Carbon nanotube transistor operation at 2.6 GHz. *Nano Lett.* **4,** 753–756 (2004).
89. Li, S. D., Yu, Z., Rutherglen, C. & Burke, P. J. Electrical properties of 0.4 cm long single-walled carbon nanotubes. *Nano Lett.* **4,** 2003–2007 (2004).
90. Park, J. Y. *et al.* Electron-phonon scattering in metallic single-walled carbon nanotubes. *Nano Lett.* **4,** 517–520 (2004).
91. Hong, B. H. *et al.* Quasi-continuous growth of ultralong carbon nanotube arrays. *J. Am. Chem. Soc.* **127,** 15336–15337 (2005).
92. Purewal, M. S. *et al.* Scaling of resistance and electron mean free path of single-walled carbon nanotubes. *Phys. Rev. Lett.* **98,** 186808 (2007).
93. Javey, A., Guo, J., Wang, Q., Lundstrom, M. & Dai, H. J. Ballistic carbon nanotube field-effect transistors. *Nature* **424,** 654–657 (2003).
94. Javey, A., Qi, P. F., Wang, Q. & Dai, H. J. Ten- to 50-nm-long quasi-ballistic carbon nanotube devices obtained without complex lithography. *Proc. Natl Acad. Sci. USA* **101,** 13408–13410 (2004).
95. Javey, A. *et al.* High-field quasiballistic transport in short carbon nanotubes. *Phys. Rev. Lett.* **92,** 106804 (2004).
96. Snow, E. S., Novak, J. P., Campbell, P. M. & Park, D. Random networks of carbon nanotubes as an electronic material. *Appl. Phys. Lett.* **82,** 2145–2147 (2003).
97. Zhou, Y. *et al.* P-channel, n-channel thin film transistors and p–n diodes based on single wall carbon nanotube networks. *Nano Lett.* **4,** 2031–2036 (2004).
98. Ozel, T., Gaur, A., Rogers, J. & Shim, M. Polymer electrolyte gating of carbon nanotube network transistors. *Nano Lett.* **5,** 905–911 (2005).
99. Hur, S. *et al.* Printed thin-film transistors and complementary logic gates that use polymer-coated single-walled carbon nanotube networks. *J. Appl. Phys.* **98,** 114302 (2005).
100. Cao, Q. *et al.* Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature* **454,** 495–500 (2008).
101. Ishikawa, F. N. *et al.* Transparent electronics based on transfer printed aligned carbon nanotubes on rigid and flexible substrates. *ACS Nano* **3,** 73–79 (2009).
102. Kocabas, C., Kang, S. J., Ozel, T., Shim, M. & Rogers, J. A. Improved synthesis of aligned arrays of single-walled carbon nanotubes and their implementation in thin film type transistors. *J. Phys. Chem. C* **111,** 17879–17886 (2007).
103. Cao, Q., Xia, M., Shim, M. & Rogers, J. Bilayer organic-inorganic gate dielectrics for high-performance, low-voltage, single-walled carbon nanotube thin-film transistors, complementary logic gates, and p–n diodes on plastic substrates. *Adv. Funct. Mater.* **16,** 2355–2362 (2006).
104. Snow, E. S., Campbell, P. M., Ancona, M. G. & Novak, J. P. High-mobility carbon-nanotube thin-film transistors on a polymeric substrate. *Appl. Phys. Lett.* **86,** 033105 (2005).
105. Kanungo, M., Lu, H., Malliaras, G. & Blanchet, G. Suppression of metallic conductivity of single-walled carbon nanotubes by cycloaddition reactions. *Science* **323,** 234–237 (2009).
106. Bao, Z. & Locklin, J. J. *Organic Field-Effect Transistors* (CRC Press, 2007).
107. Noh, Y. Y., Zhao, N., Caironi, M. & Sirringhaus, H. Downscaling of self-aligned, all-printed polymer thin-film transistors. *Nature Nanotech.* **2,** 784–789 (2007).
108. Subramanian, V. *et al.* Progress toward development of all-printed RFID tags: Materials, processes, and devices. *Proc. IEEE* **93,** 1330–1338 (2005).
109. Rutherglen, C. & Burke, P. Carbon nanotube radio. *Nano Lett.* **7,** 3296–3299 (2007).
110. Jensen, K., Weldon, J., Garcia, H. & Zettl, A. Nanotube radio. *Nano Lett.* **7,** 3508–3511 (2007).
111. O, K. *et al.*, On-chip antennas in silicon ICs and their application. *IEEE Trans. Electron Dev.* **52,** 1312–1323 (2005).
112. Burke, P. J., Li, S. D. & Yu, Z. Quantitative theory of nanowire and nanotube antenna performance. *IEEE Trans. Nanotech.* **5,** 314–334 (2006).
113. Hanson, G. W. Fundamental transmitting properties of carbon nanotube antennas. *IEEE Trans. Antenn. Propag.* **53,** 3426–3435 (2005).
114. Burke, P. & Rutherglen, C. Towards a single-chip, implantable RFID system: Is a single-cell radio possible? *Biomed. Microdevices* doi:10.1007/s10544-008-9266-4 (2009).
115. Farmer, D. B. *et al.* Utilization of a buffered dielectric to achieve high field-effect carrier mobility in graphene transistors. *Nano Lett.* doi:10.1021/nl902788u (2009).

Acknowledgements

This work was funded by the National Science Foundation, the Army Research Office, the Office of Naval Research, Northrop Grumman and the Korean National Science Foundation (KOSEF) World Class University (WCU) programme.

Additional information

The authors declare competing financial interests: details accompany the paper at www.nature.com/naturenanotechnology.